

LAYER 1 : TOP
LAYER 2 : GND1
LAYER 3 : IN1
LAYER 4 : VCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : GND2
LAYER 8 : BOT

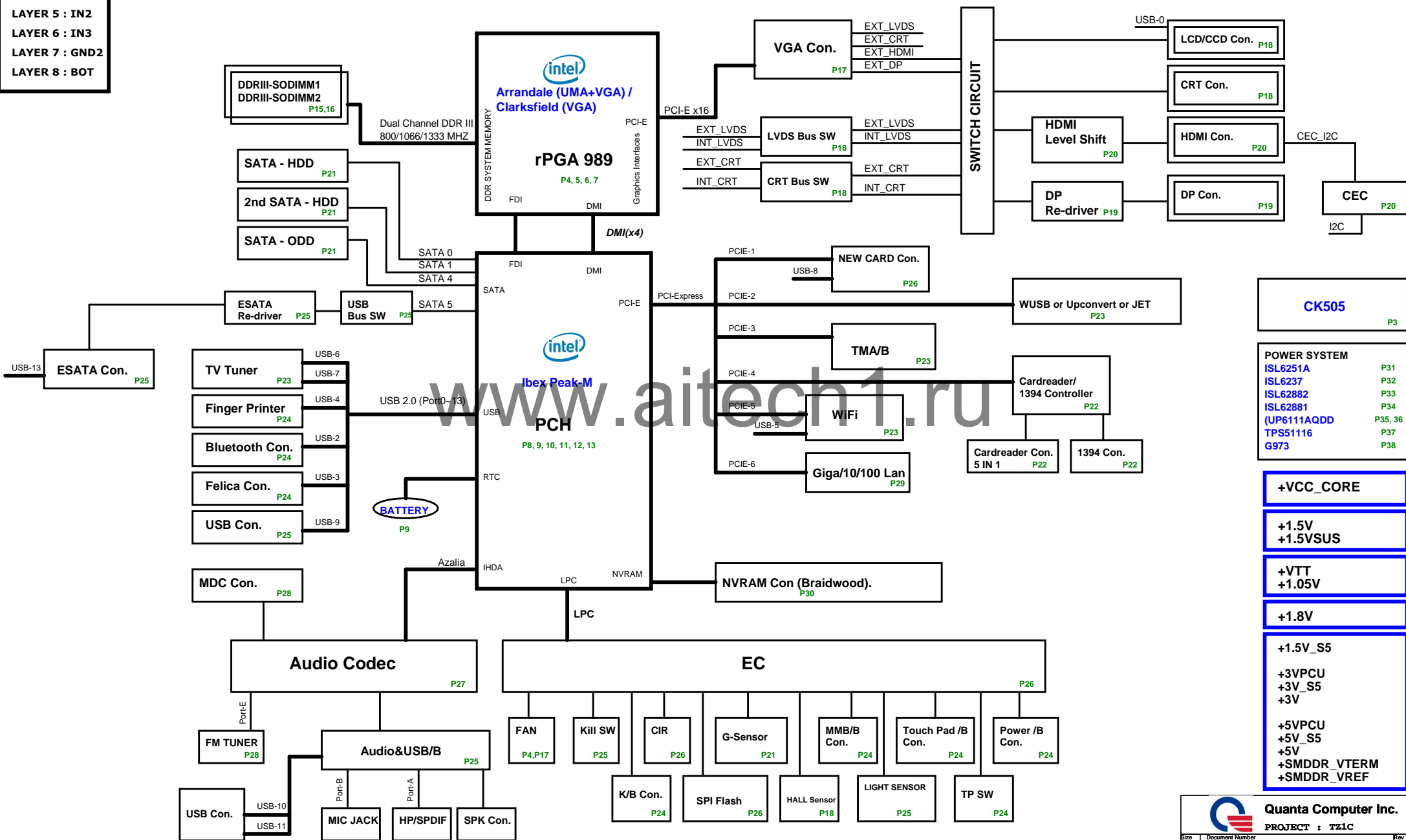


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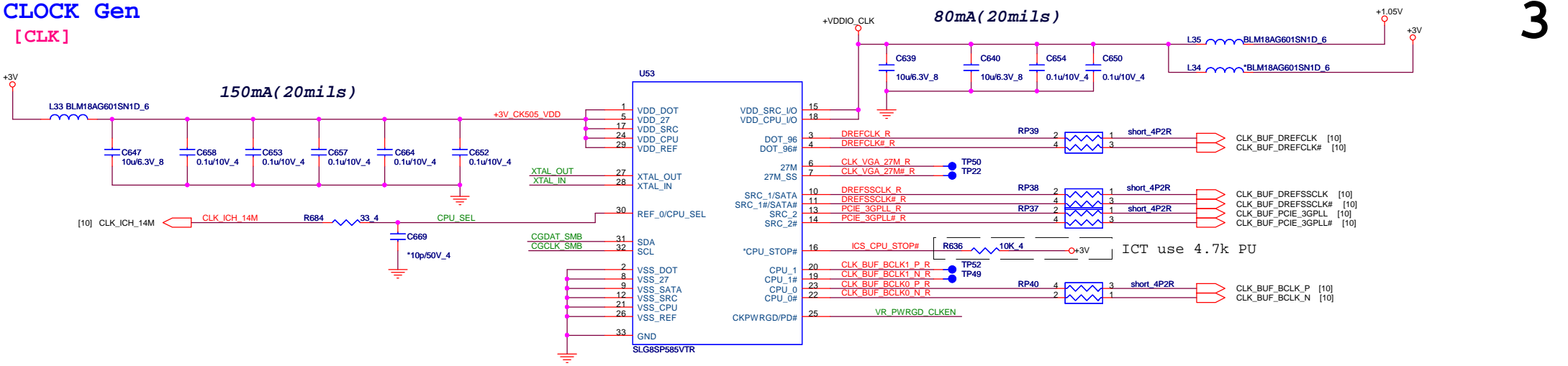
PAGE	DESCRIPTION	BOI-FUNCTIONS
1	Schematic Block Diagram	
2	Front Page	
3	Clock Generator	CLK
4-7	Processor	CPU
8-14	PCH	CLG
9	RTC	RTC
15-16	DDRIII SO-DIMM	DDR
17	VGA Connector	VGA
18	LCD Panel	LDS
	CRT & CRT BUS SWITCH	CRT
	CCD	CCD
	HALL SENSOR&BACK LIGHT SWITCH	HSR
19	Display Port	DPP
20	HDMI comm part	HDM
	HDMI for GM	HMG
21	SATA ODD	ODD
	Main SATA HDD & 2nd SATA HDD	HDD
	G-Sensor	H3D
22	5 IN 1 Card reader	MMC
	IEEE1394	FIW
23	MINI Card (Wi-Fi & WIMAX)	WLN
	MINI Card 2nd	MNC
	MINI Card 3rd	MNC
	TMA Connector	TMA
24	INT KeyBoard & K/B LED Power	KBC
	LED Board	LED
	TP&FP board	TPD,FPD
	Bluetooth Connector	BTM
	Felica Connector	FEC
	MMB Connector	MMB
	Power SW	PSW
	B-CAS Connector	BCS
25	New Card (Express Card)	EXC
	E-SATA comb USB	ESA
	USB Connector	USB
	Audio & USB Board	USB,ADO
	Light Sensor	LSN
	Satellite LED	LED
	RF LED / WIMAX LED / Kill SW	KSW
26	EC WP8763LDG/WPC8769L(O)	KBC
	CIR	CIR
27	Codec (CX20583)	ADO
28	FM Tunner	FMM
	Modem Connector	MDM
	HOLE	
29	Atheros LAN	LAN
30	NVRAM Connecyor	NVR
31	Charger (ISL6251A)	PWM
32	System 5V/3V (ISL6237)	PWM
33	CPU CORE (ISL62882)	PWM

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0~S5
+VCCRTC	+3.0V~+3.3V		S0~S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
+5V_TMA	+5V	MAIN_ON	S0
WIMAX_P	+3.3V	WMAX_P for EC	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_S5	+1.5V	S5_ON	S0~S5
+1.5V_SUS	+1.5V	SUSON	S0~S3
+VCC_CORE		VRON	S0
+VTT	+1.05V~+1.1V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		GFXVR_EN	S0

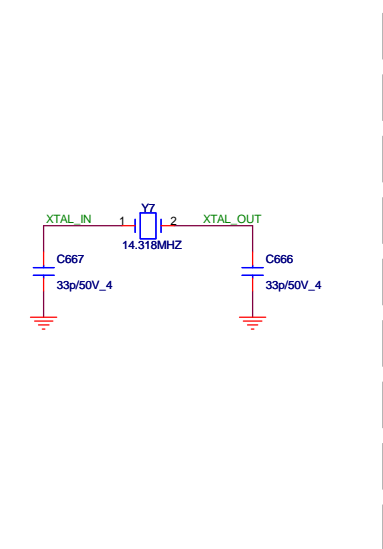
GND PLANE	PAGE
⏚ GND_SIGNAL	32
⏚ CARD_GND	21
⏚ AGND_DC/DC	31
⏚ GND	ALL

PAGE	DESCRIPTION	BOI-FUNCTIONS
34	VAXG (ISL62881)	PWM
35	+VTT (UP6111A)	PWM
36	+1.05V (UP6111AQDD)	PWM
37	DDR 1.5V (TPS51116)	PWM
38	Discharge (1.5V_S5/1.8V)	PWM
39	Power Tree Table	
40	PCH Power Plane	
41	Power Management	
42	Change List	

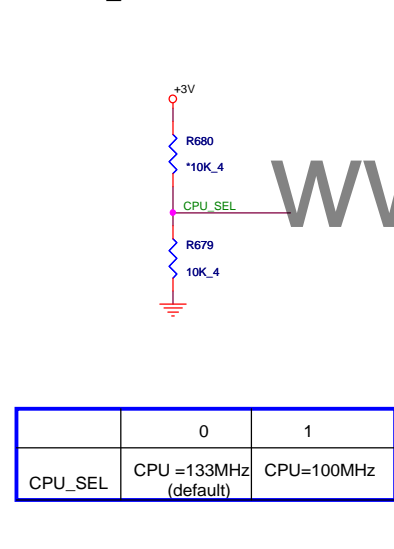
CLOCK Gen
[CLK]



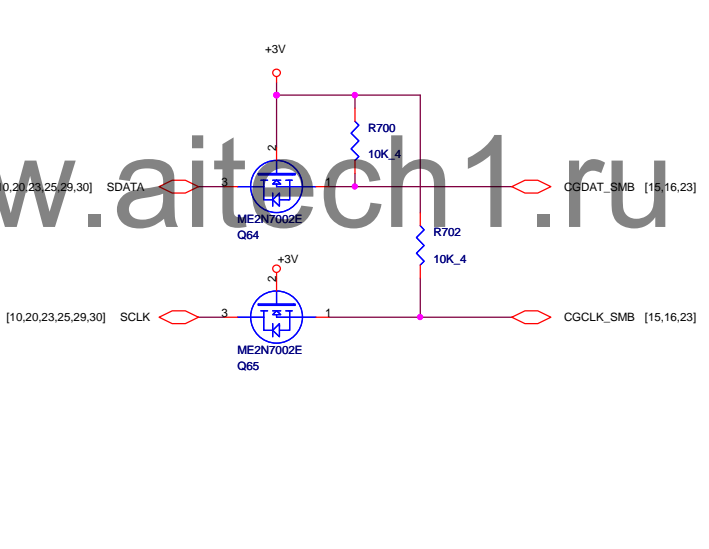
CLK CRYSTAL



CLK CPU_SEL

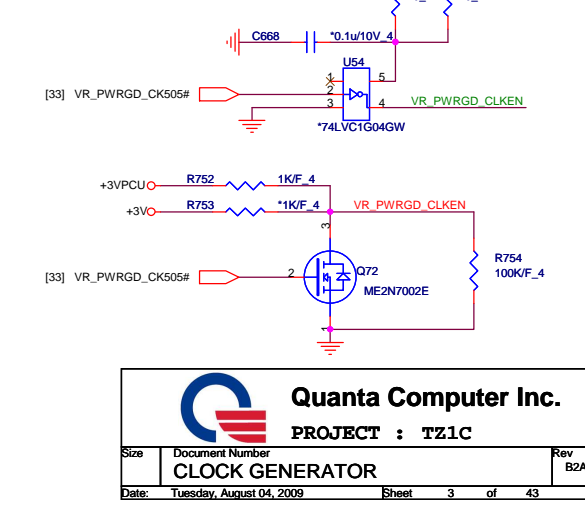


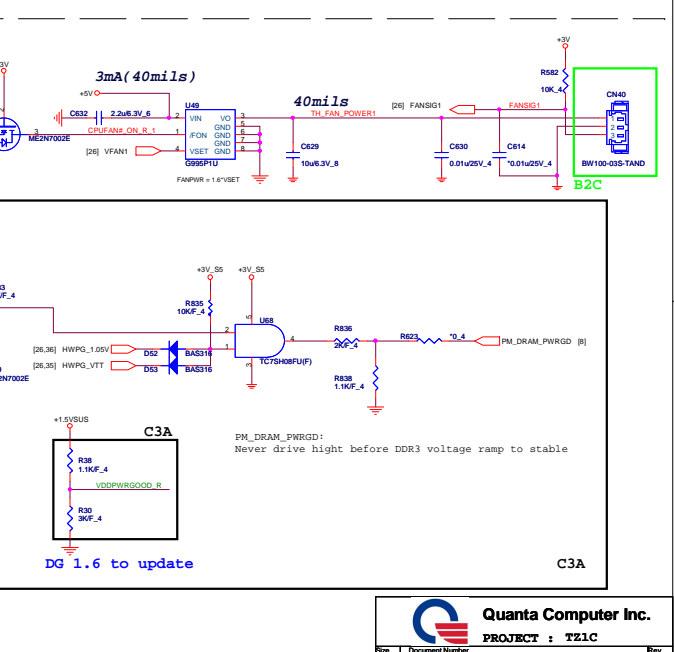
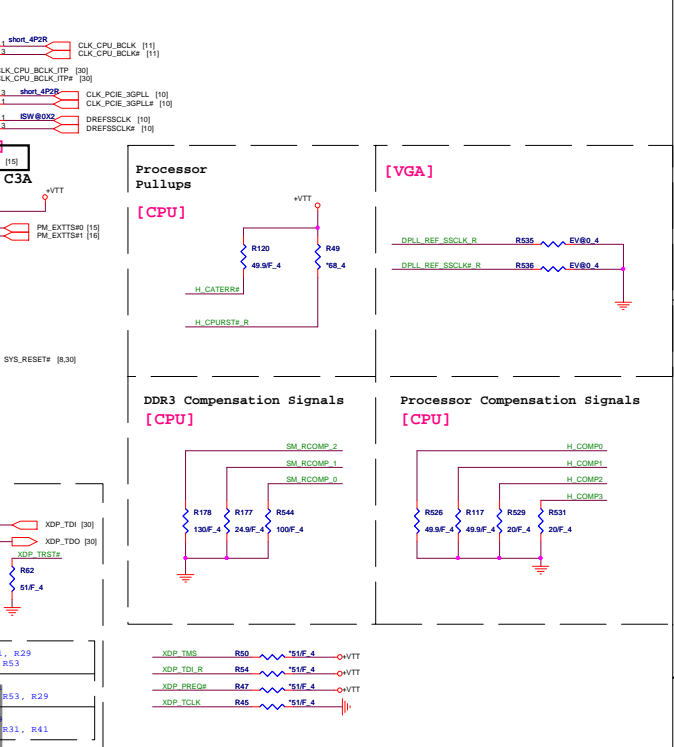
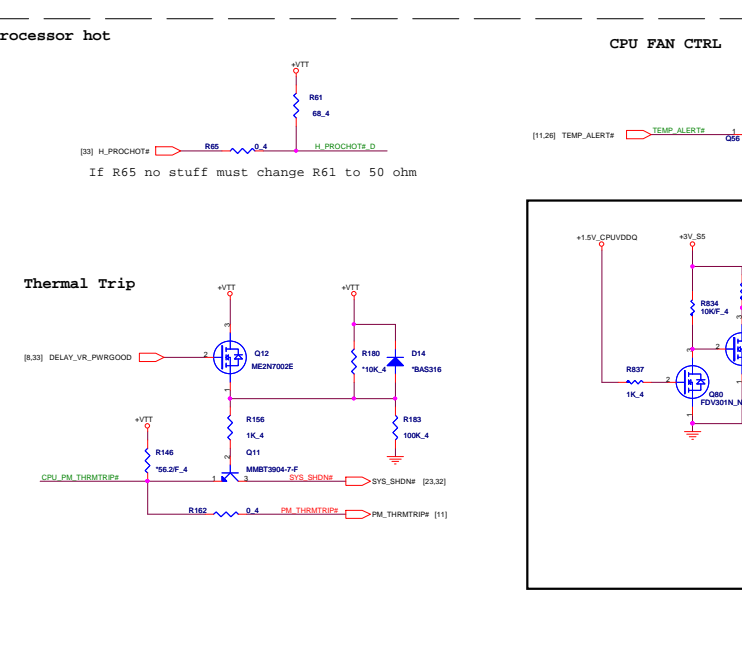
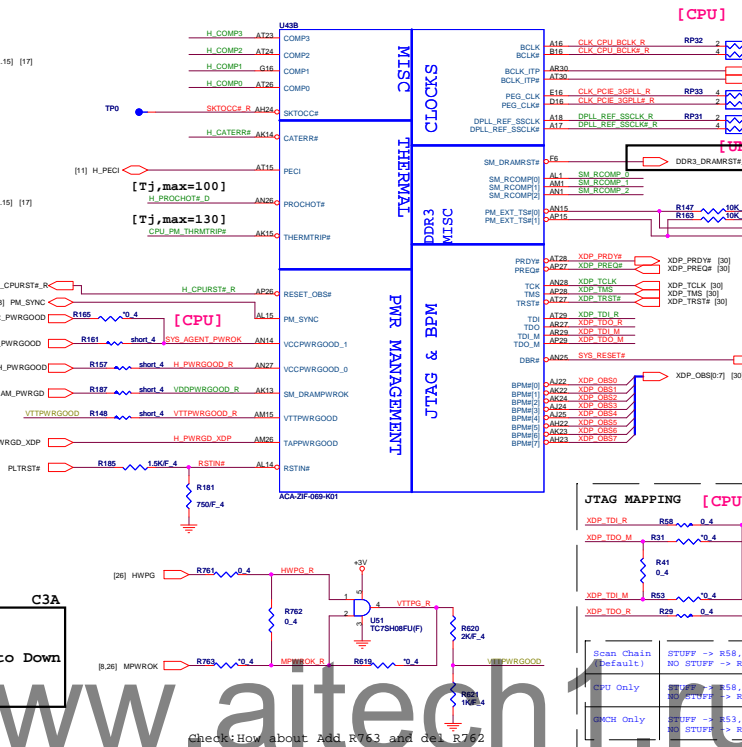
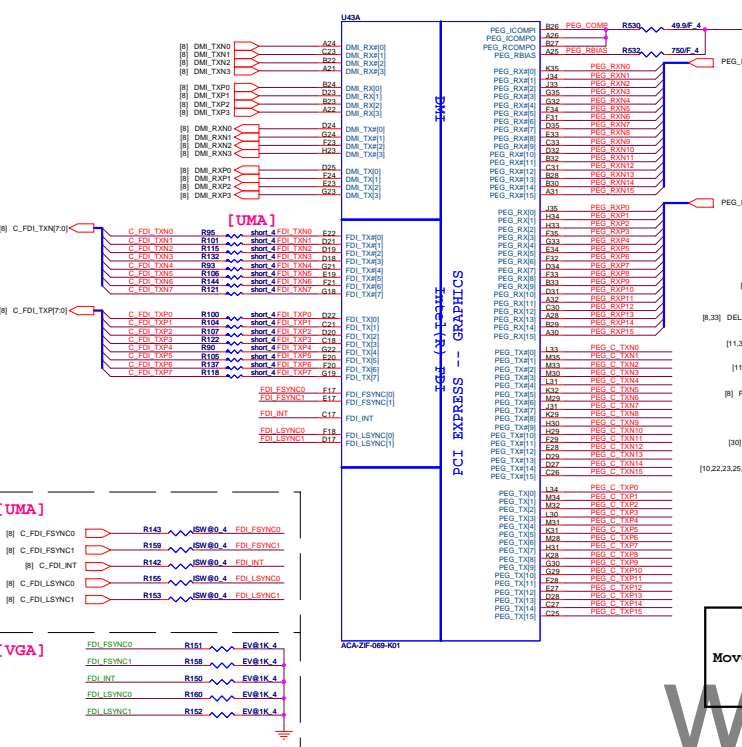
CLK I2C



CLK POWERGOOD

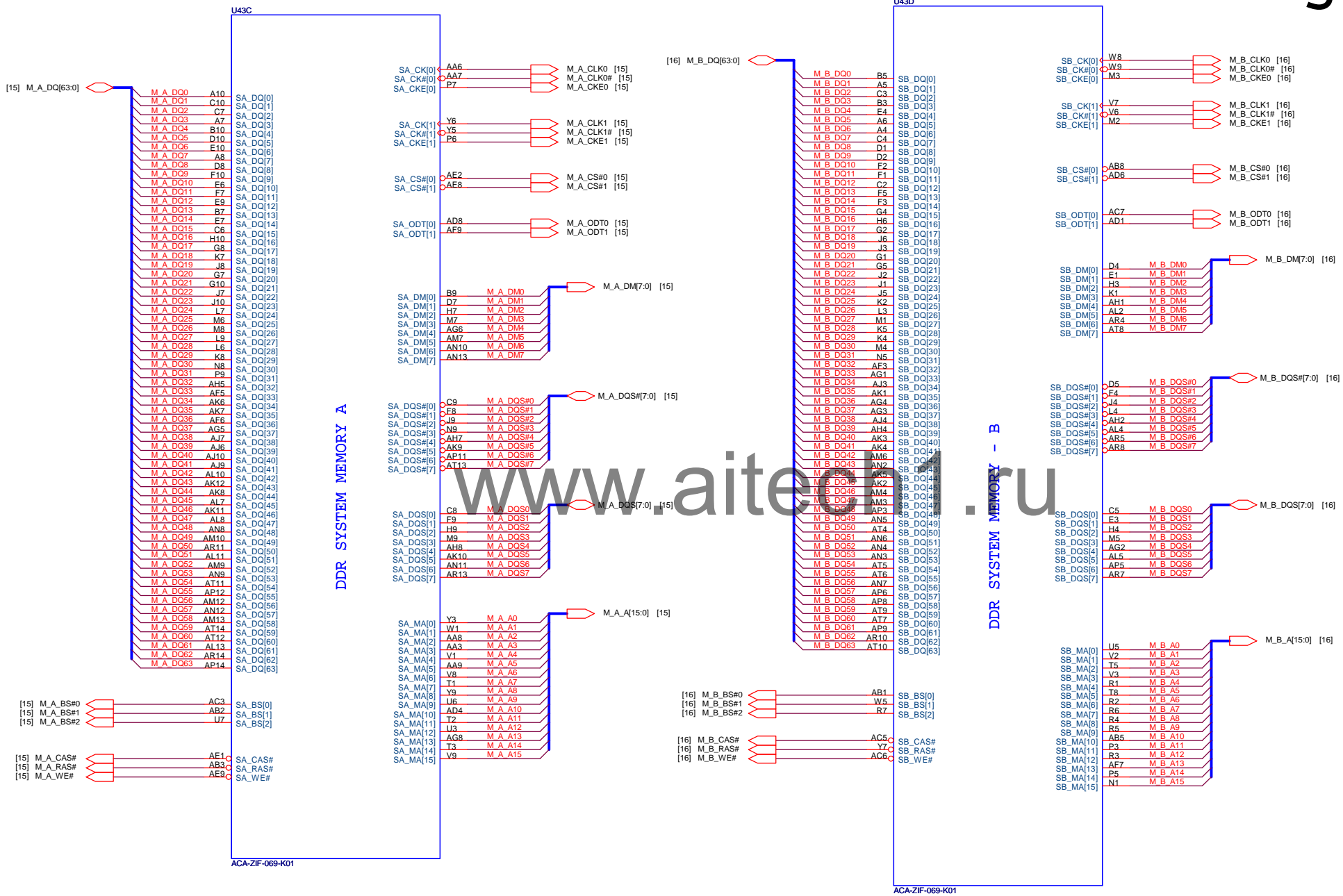
Change to +3VPCU
(follow CRB)



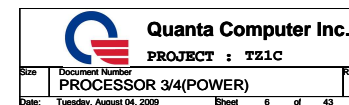


AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

5

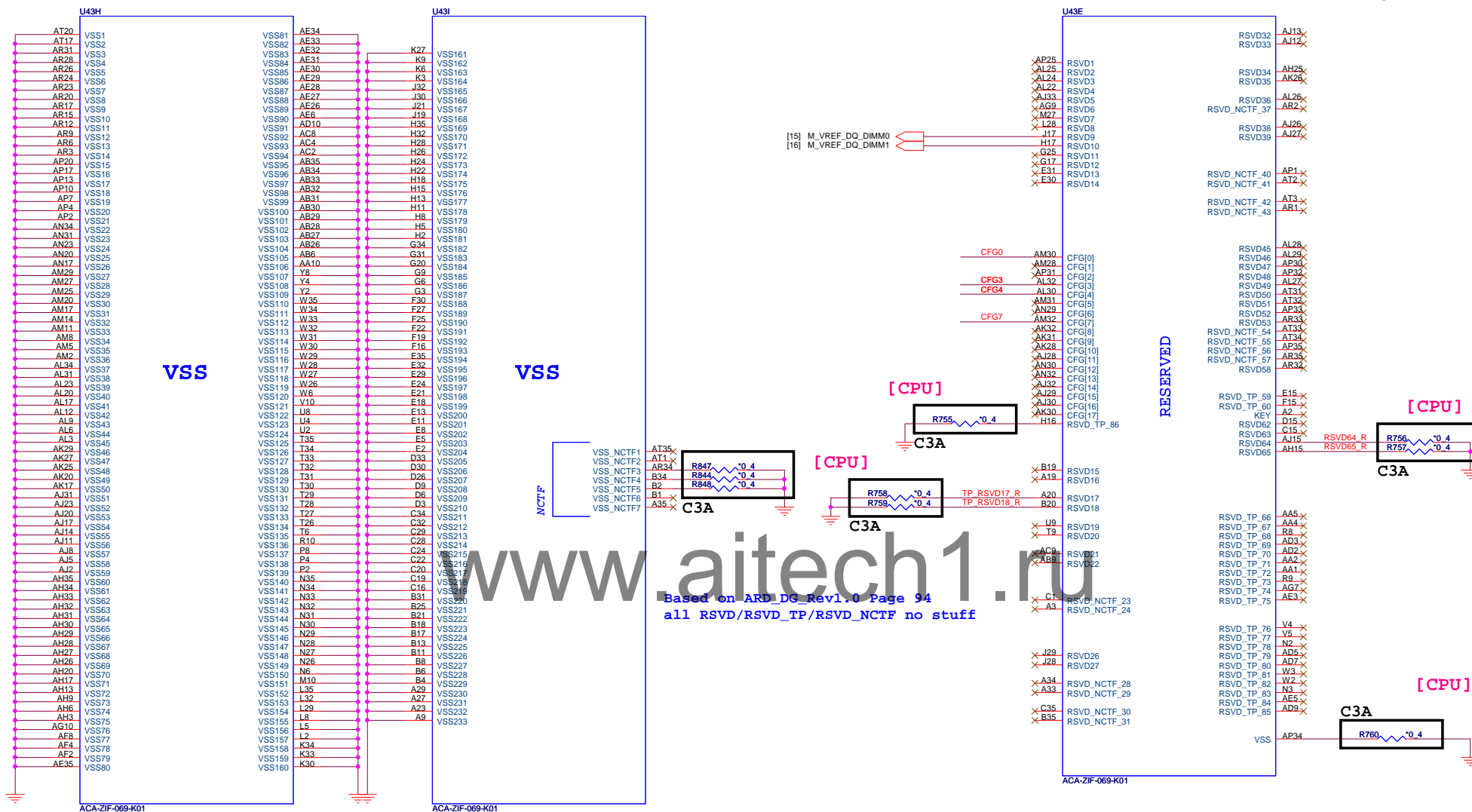


AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)



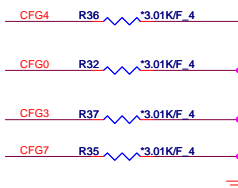
[CPU] AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



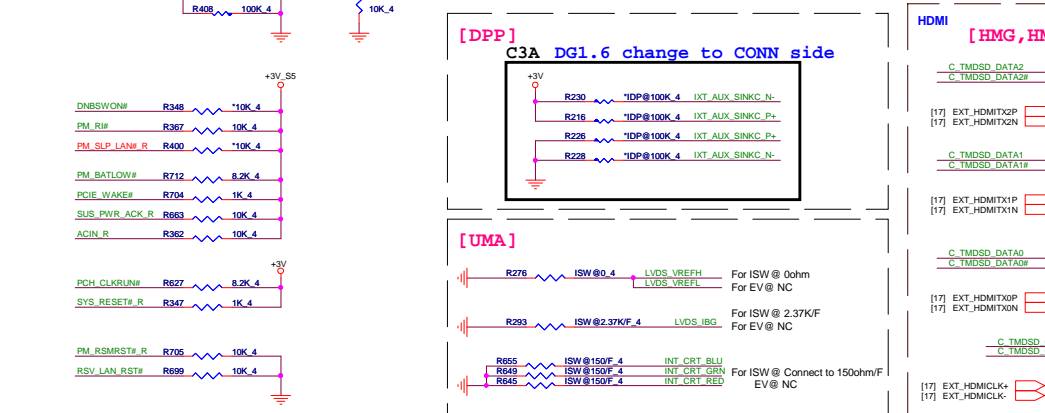
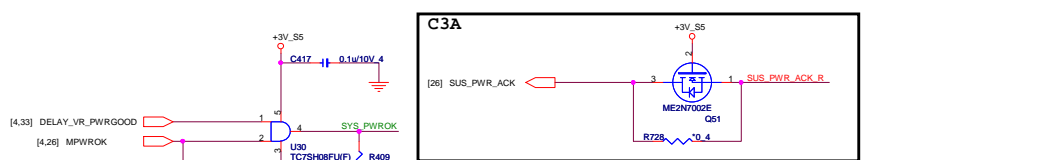
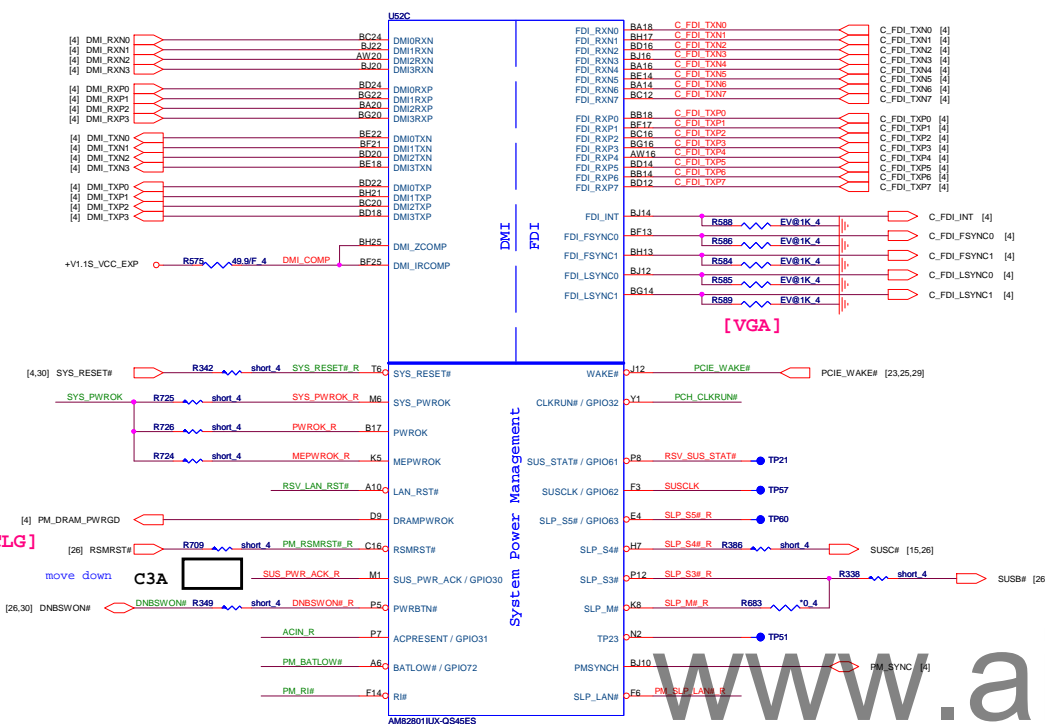
Processor Strapping

	1	0	DEFAULT
CFG4 (Embended Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port	1
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled	1
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed	1

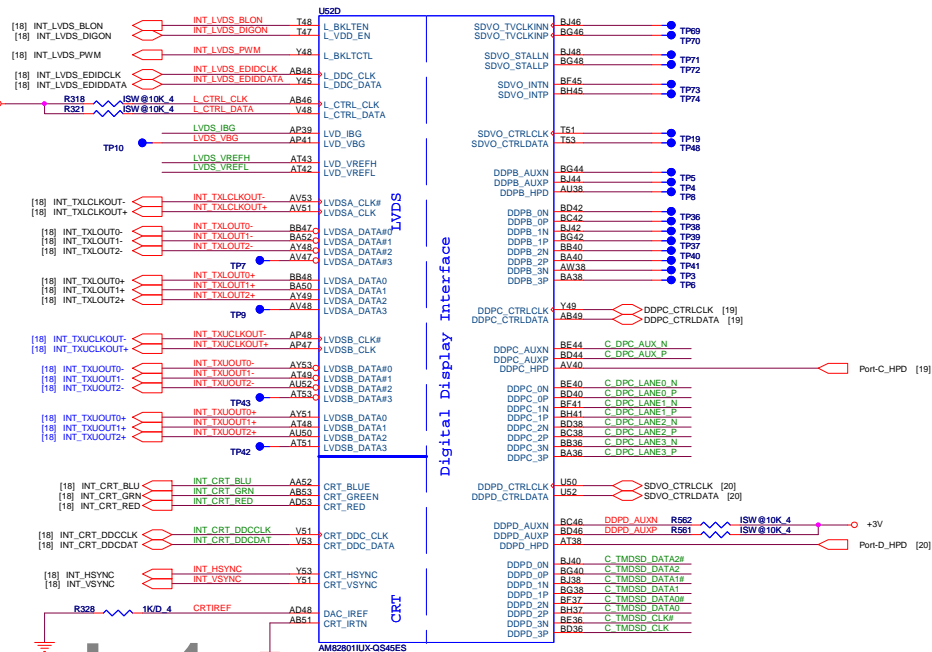


Both FDI and DMI Supports Lane Reversal but only at PCH side enable via PCH soft strap

IBEX PEAK-M (LVDS,DDI)

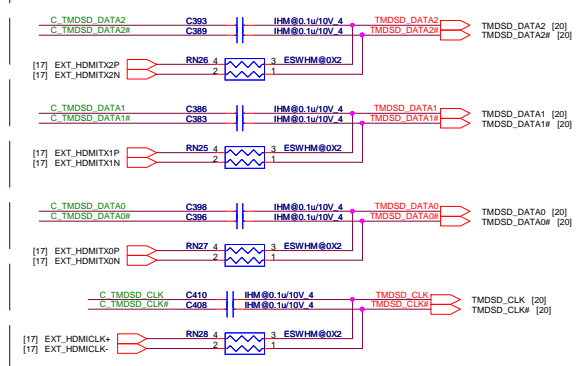


LVDS IF

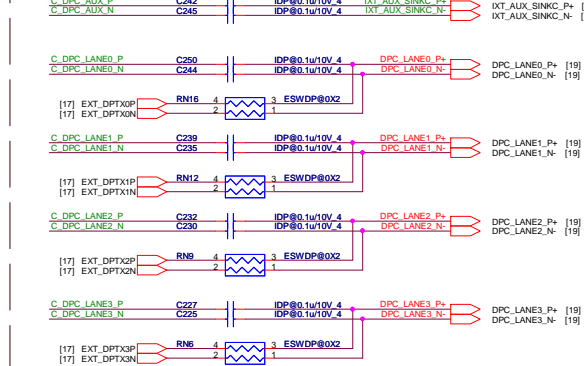


Port	Strap	How to enable Port?	How to disable Port?
LVDS	L_DPC DATA	PU to 3.3V with 2.2k+/- 5%	NC
Port B	SDVO_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port C	DDPC_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
Port D	DDPD_CTRLDATA	PU to 3.3V with 2.2k+/- 5%	NC
eDP	CFG[4]	PD to GND directly	NC

HDMI [HMG,HMP]



Display port [DPP]

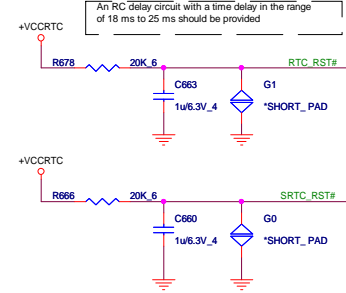


DisplayPort
Switchable: SW+DP and ESWD
VGA: EDP
UMA: IDP

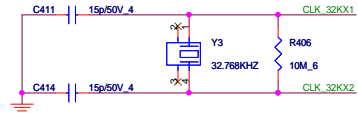
HDMI
Switchable: SW+HM and ESWHM
VGA: EHM
UMA: IHM

[CLG]

RESET JUMP

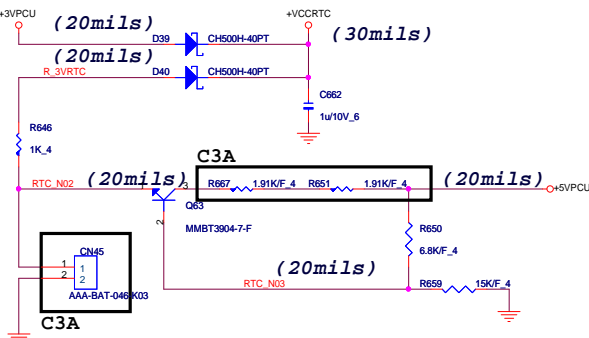


RTC CRYSTAL

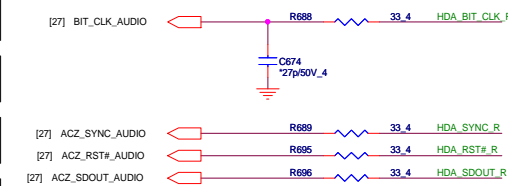


[RTC]

RTC BATTERY



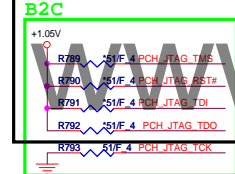
HD Audio I/F



IBEX PEAK-M (HDA,JTAG,SATA) [HM55 can not use SATA port2,3]

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C3A



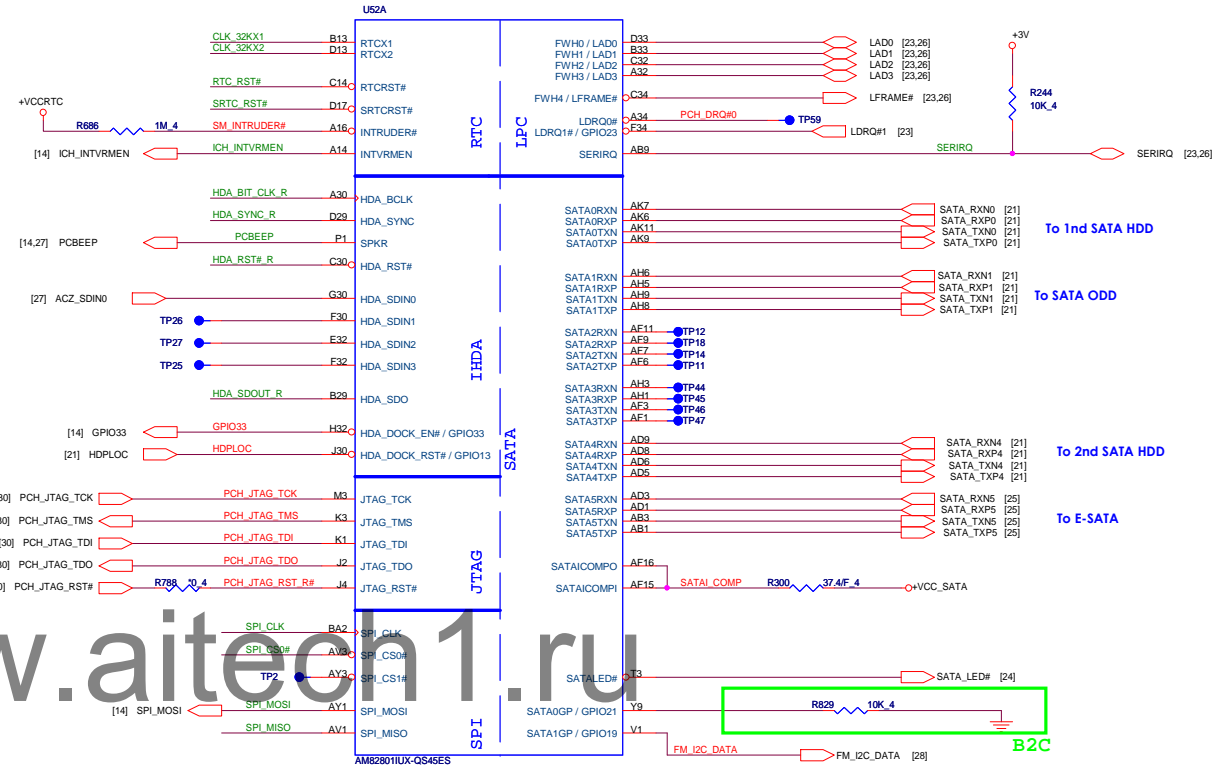
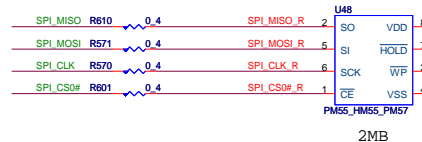
Note:Based on WW11 MoW.
only R793 default stuff others no stuff

[BIOS&ME]

Default PM55 for clarksfield

Winbond: 8MB/SOIC8-->[W25Q64BVSSIG]
4MB/SOIC8-->[W25X40AVSSIG]
2MB/SOIC8-->[W25Q16AVSSIG]

BOM :must different with U45



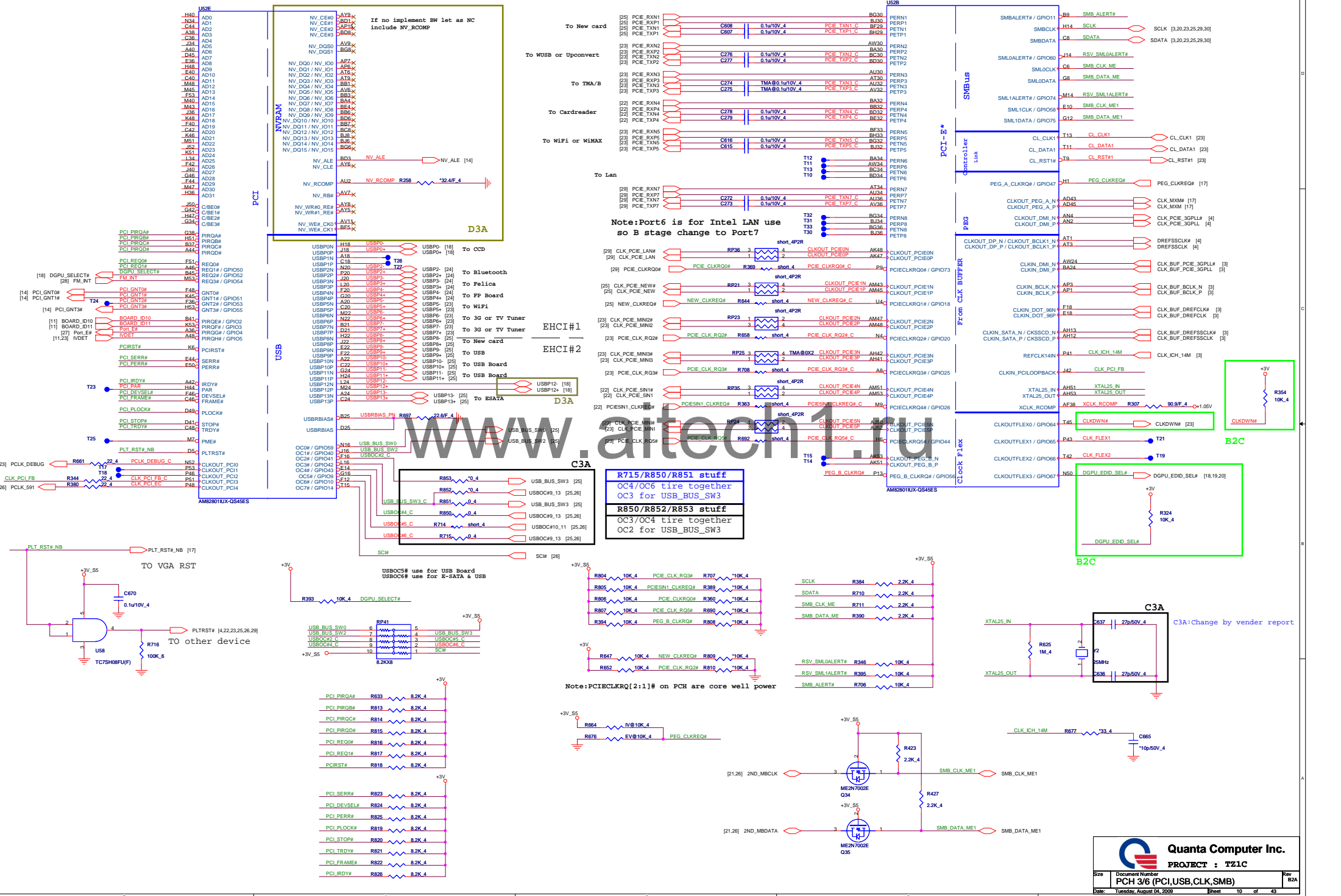
PCH	2MB	4MB	8MB
PM55	●		
HM55			
HM57 / PM57		●	●
QM57 / QS57			●

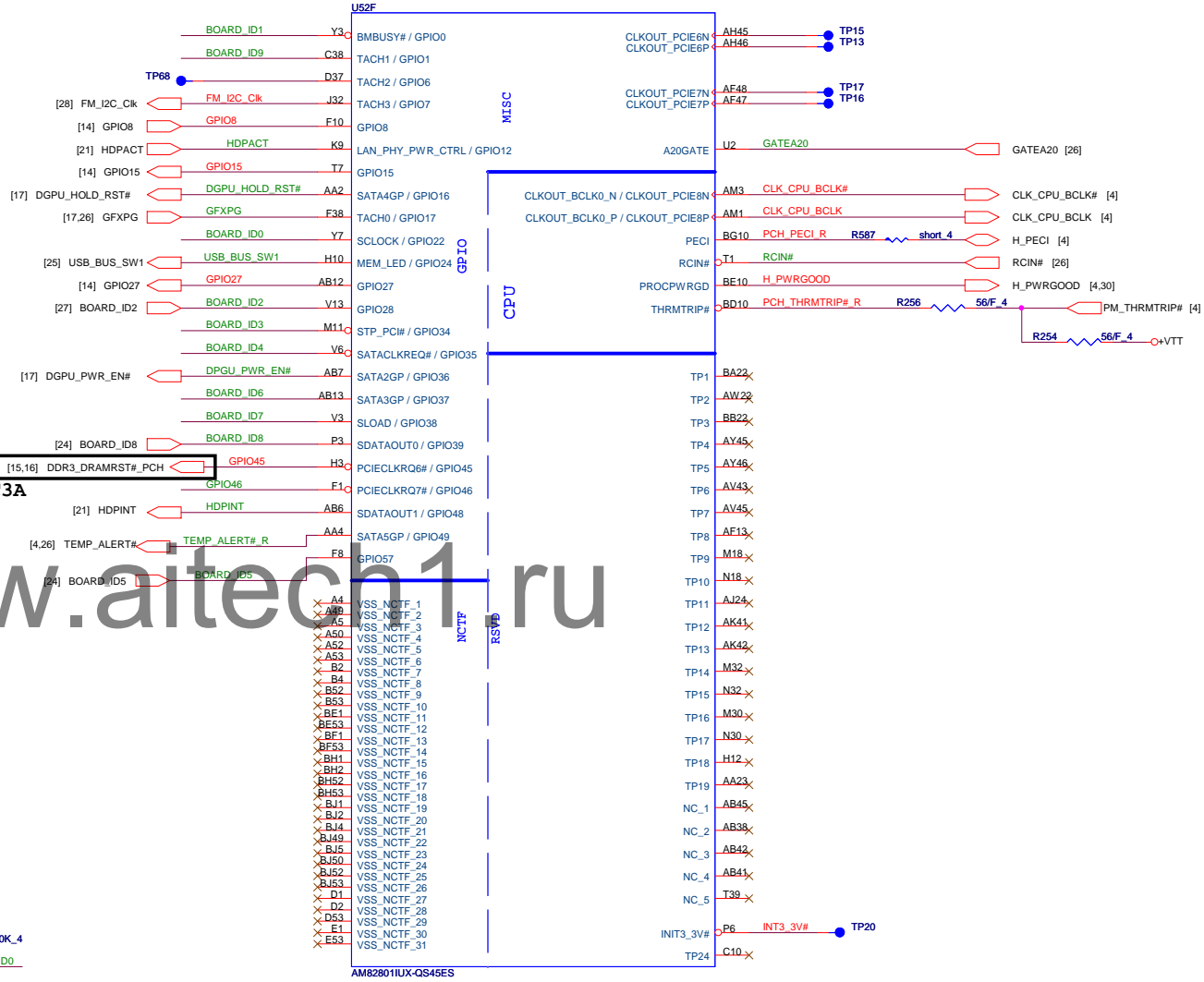
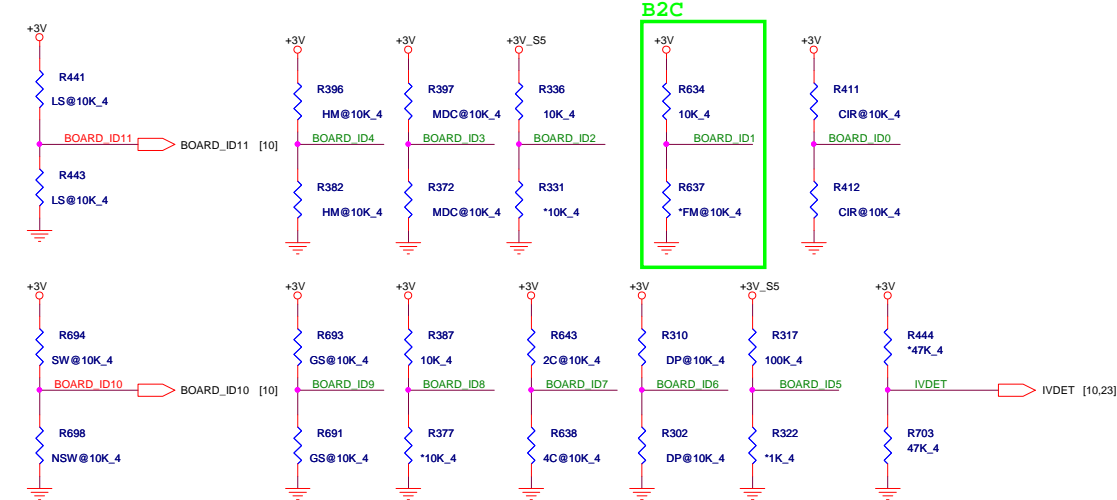
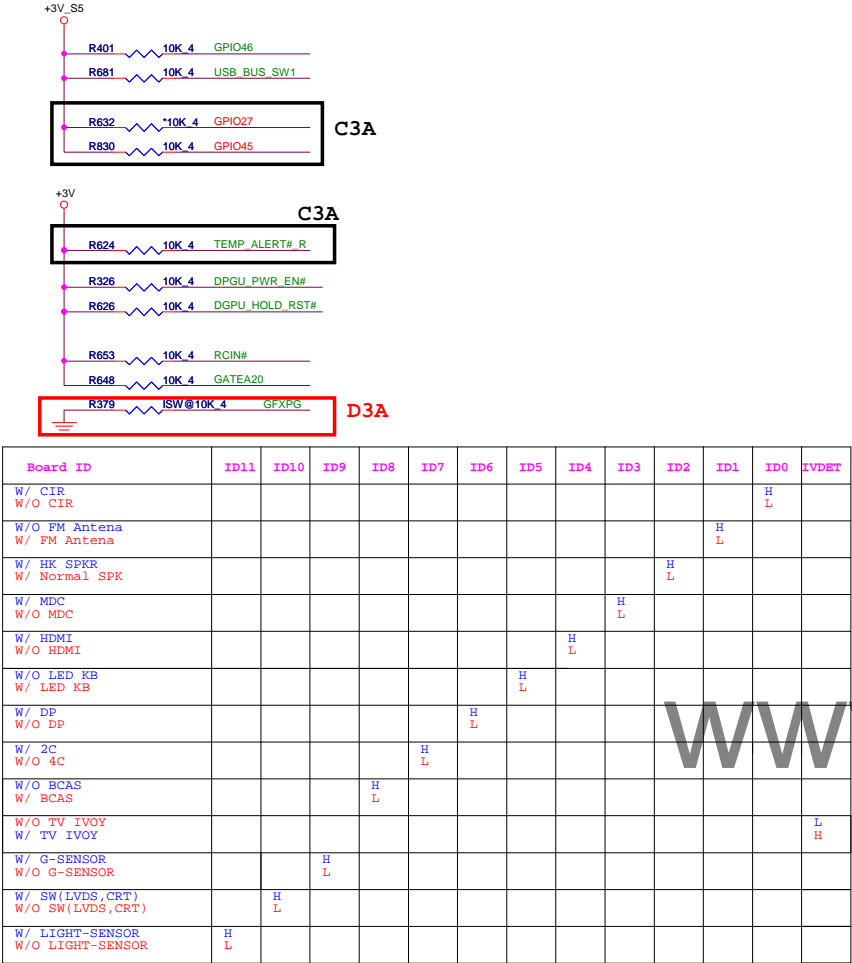
Quanta Computer Inc.
PROJECT : TZ1C

Size: Document Number: PCH 2/6 (SATA,LPC,SPI,HD) Rev: B2A

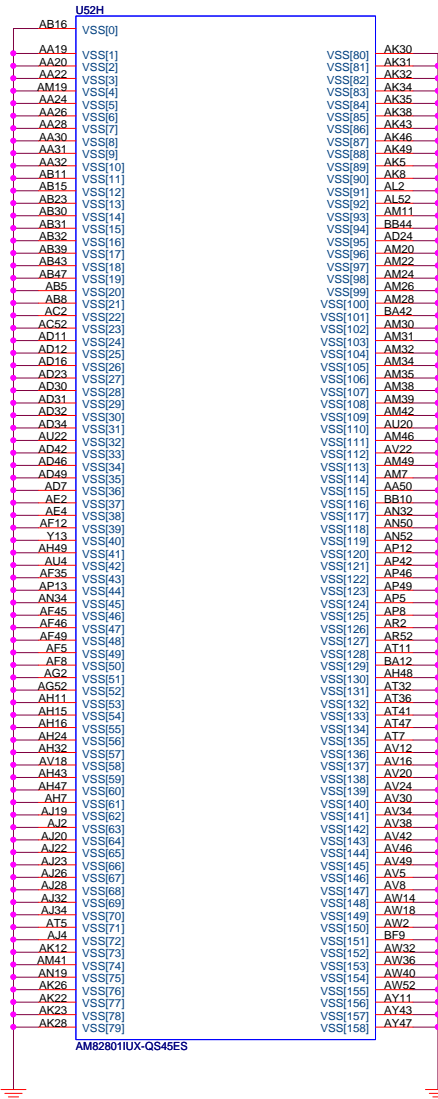
Date: Tuesday, August 04, 2009 Sheet: 9 of 43

IBEX PEAK-M (PCI,USB,NVRAM)
[HM55 can not use USB port6,7]






IBEX PEAK-M (GND)



AM82801IUX-QS45ES








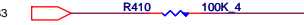





AM82801IUX-QS45ES




Quanta Computer Inc.
PROJECT : TZ1C

Size	Document Number	Rev
	PCH 6/6 (GND)	B2A
Date:	Monday, May 11, 2009	Sheet 13 of 43

Pin Name	Strap description	Configuration	Setting	when sampled
SPKR	Reboot option at power-up	0 = Default Mode (Internal weak Pull-down) 1 = No Reboot Mode with TCO Disabled	[9,27] PCBEEP 	Rising edge of PWROK
INIT3_3V#	Reserved	Weak internal pull-down. Do not pull high.		Rising edge of PWROK
GNT3#/GPIO55	Top-Block Swap Override	0 = Top Block Swap Mode 1 = Default Mode (Internal pull-up)	[10] PCI_GNT3# 	Rising edge of PWROK
INTVRMEN	Integrated 1.05V VRM Enable / Disable	1 = Integrated VRM is enabled 0 = Integrated VRM is disabled	[9] ICH_INTVRMEN 	Always
GNT0#, GNT1#	Boot BIOS Strap	(0,0) = LPC (0,1) = Reserved NAND (1,0) = PCI (1,1) = SPI	[10] PCI_GNT0#  [10] PCI_GNT1# 	Rising edge of PWROK
SPI_MOSI	TPM Functionality Disable	1 = Enabled 0 = Disable	[9] SPI_MOSI 	Rising edge of MEPWROK
NV_ALE	IntelR Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable	1 = Enabled 0 = Disabled (Default)	[10] NV_ALE 	Rising edge of PWROK
NV_CLE	DMI Termination Voltage	DMI termination voltage. Weak internal pull-up. Do not pull low.		Rising edge of PWROK
HDA_DOCK_EN #GPIO33	Flash Descriptor Security Override	0 = Flash Descriptor Security will be overridden 1 = Security measure defined in the Flash Descriptor will be enabled.	[9] GPIO33 	Rising edge of PWROK
HDA_SDO	Reserved	This signal has a weak internal pull down. NOTE: This signal should not be pulled high		Rising edge of RSMRST#
GPIO8	Reserved	This signal has a weak internal pull up. NOTE: This signal should not be pulled low	[11] GPIO8 	Rising edge of RSMRST#
HDA_SYNC	Reserved	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.		Rising edge of RSMRST#
GPIO15	Reserved	0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality	[11] GPIO15 	Rising edge of RSMRST#
GPIO27	On-Die PLL Voltage Regulator	0 = Disables the VccVRM. Need to use on-board filter circuits for analog rails. 1 = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. This signal has a weak internal pull-up.	[11] GPIO27 	Rising edge of RSMRST#
GNT2#/GPIO53	ESI Strap (Server Only)	Tying this strap low configures DMI for ESI compatible operation. This signal has a weak internal pull-up.		Rising edge of PWROK

Boot BIOS Strap		
PCI_GNT0#	PCI_GNT1#	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



Quanta Computer Inc.

PROJECT : TZ1C

Size

Document Number

PCH STRAP

Rev

B2A

Date:

Tuesday, August 04, 2009

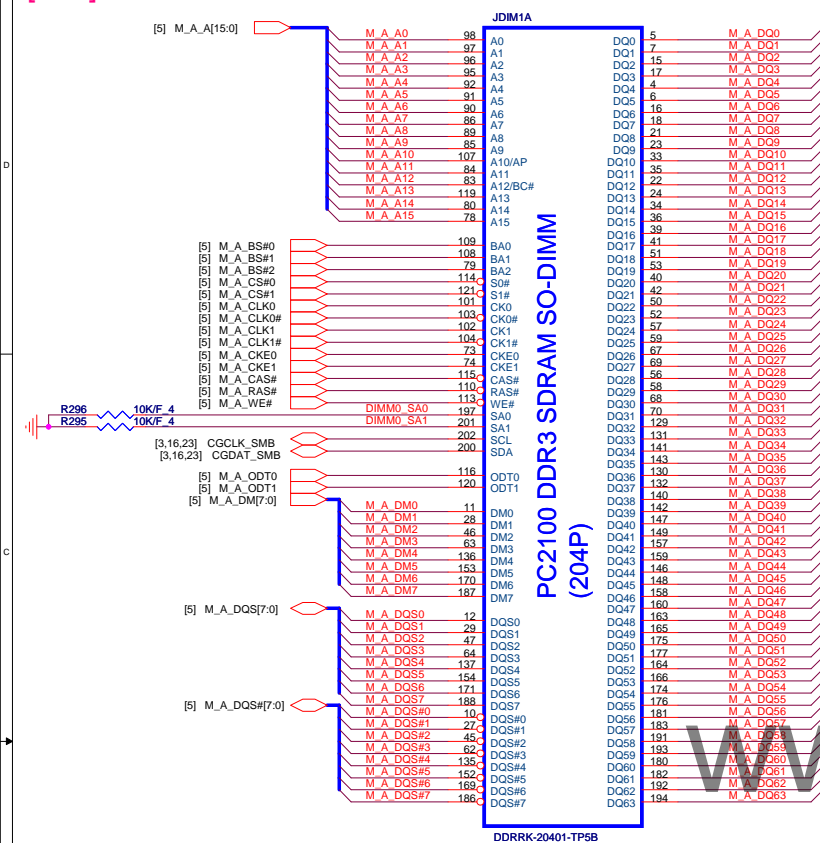
Sheet

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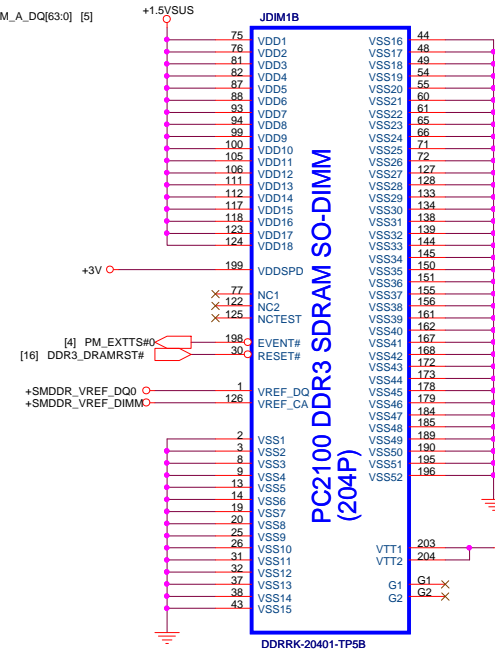
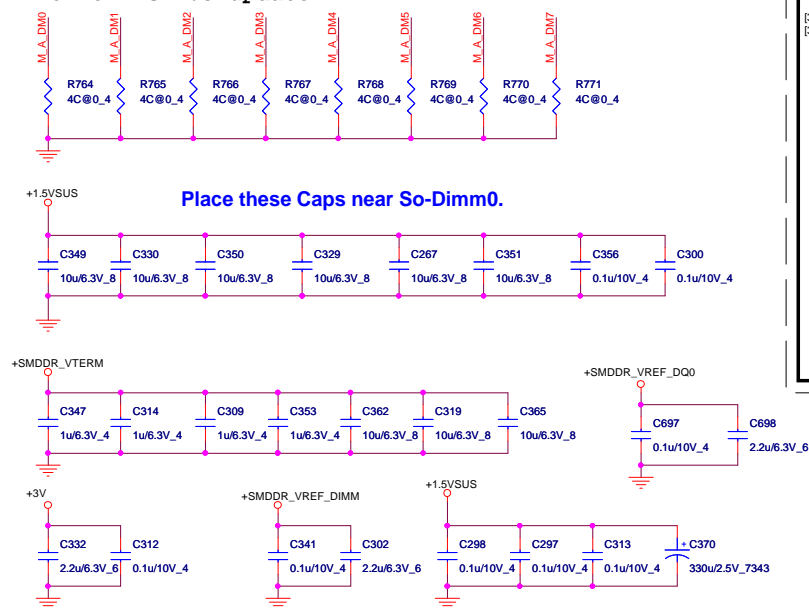
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[DDR]

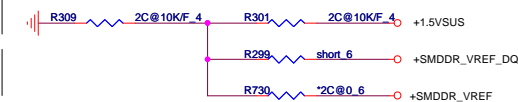


follow DG 1.5 update

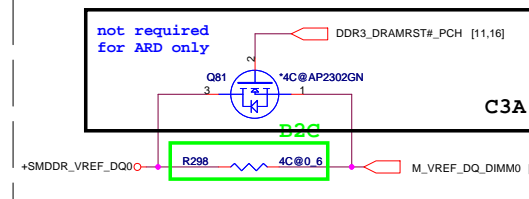


M1: Fixed SO-DIMM VREF_DQ
[Arrandale/ES/QS]

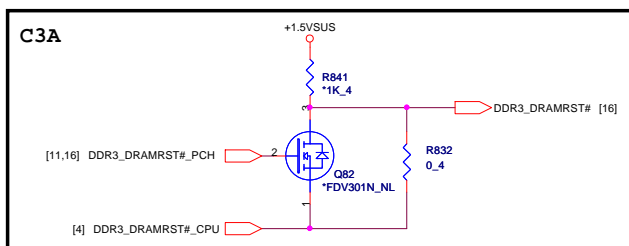
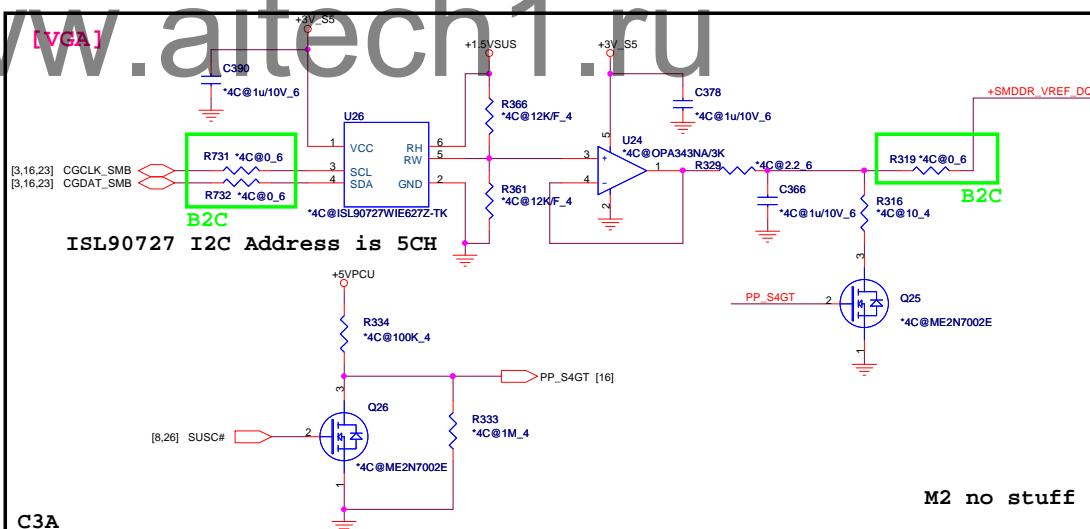
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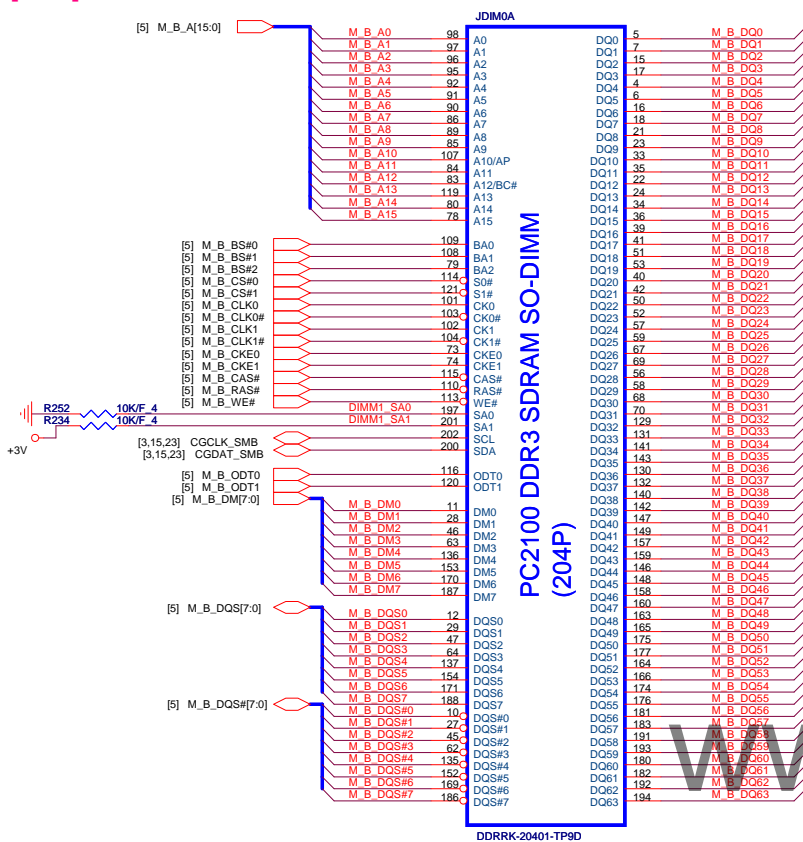
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M3:Processor Generated SO-DIMM VREF_DQ
[Clarksfield/QS]
```



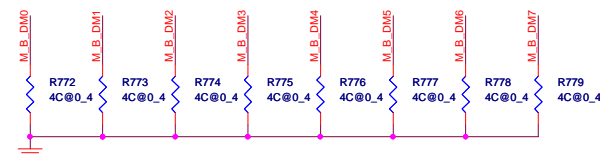
M2: Programmable SO-DIMM VREFDQ (Used for >1066MT/s)
[Clarksfield/ES]



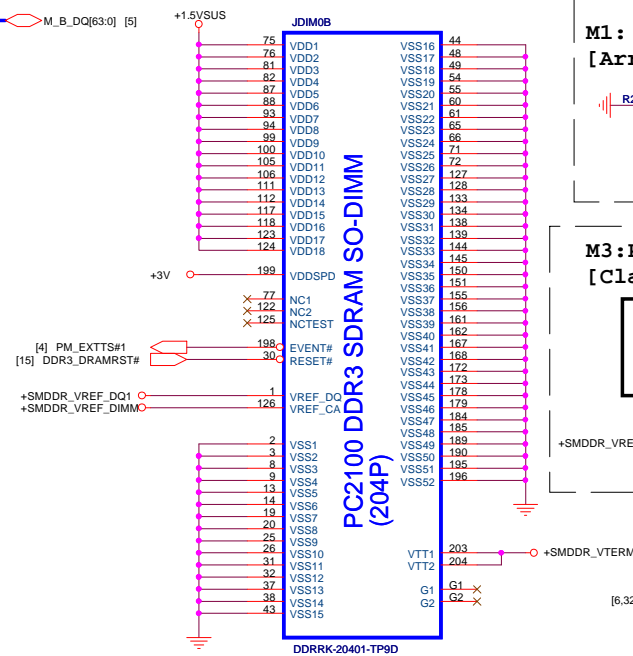
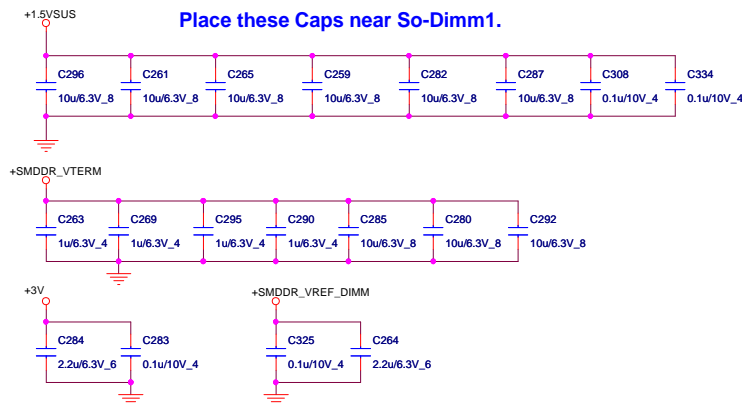
[DDR]



follow DG 1.5 update

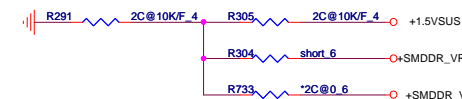


Place these Caps near So-Dimm1.

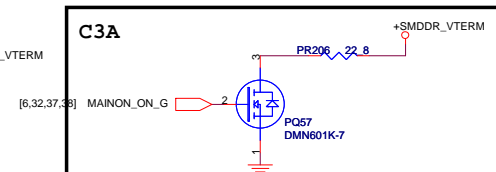
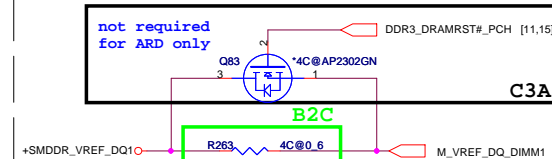


```
M1: Fixed SO-DIMM VREF_DQ
[Arrandale/ES/QS]
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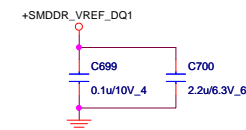
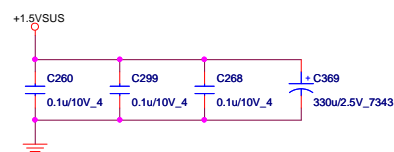
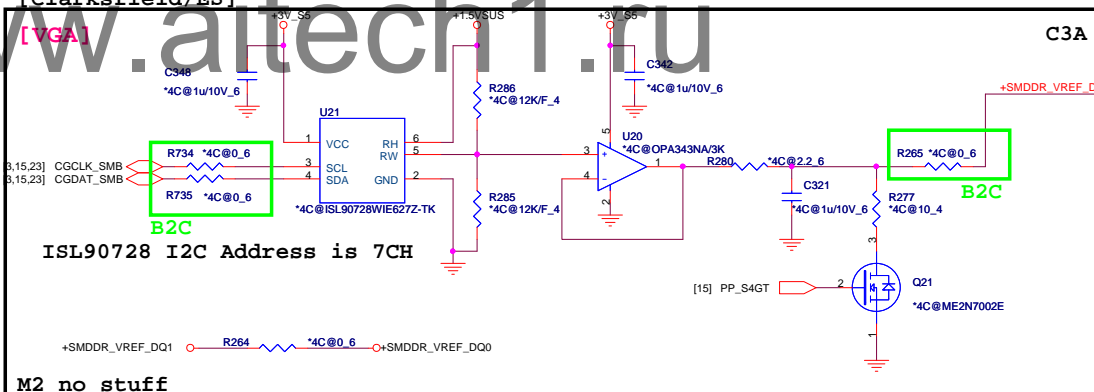
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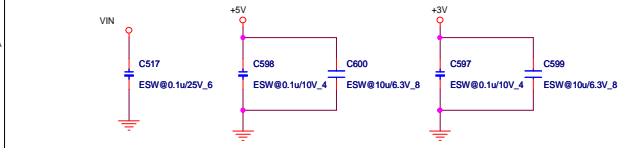
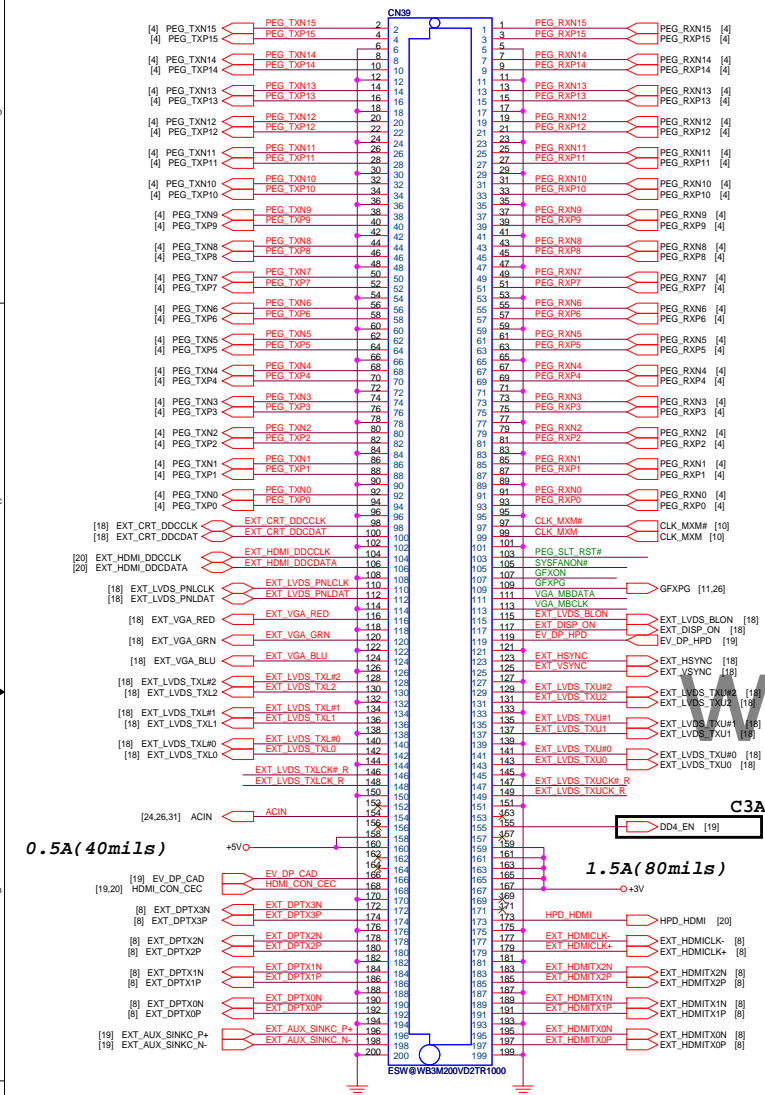
```
M3:Processor Generated SO-DIMM VREF_DQ
[Clarksfield/QS]
```



M2: Programmable SO-DIMM VREFDQ (Used for >1066MT/s)
[Clarksfield/ES]

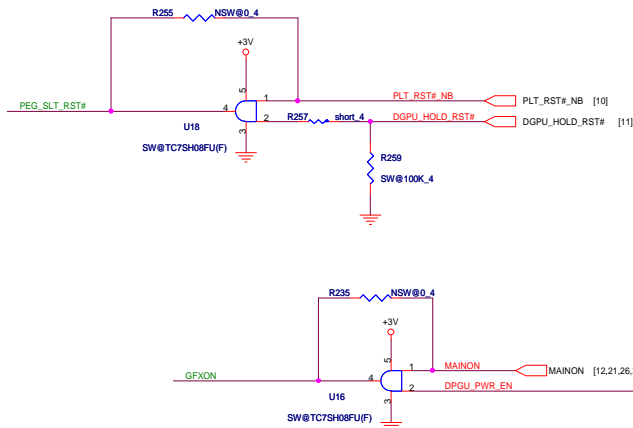


VGA BOARD CONNECOTR
[VGA]

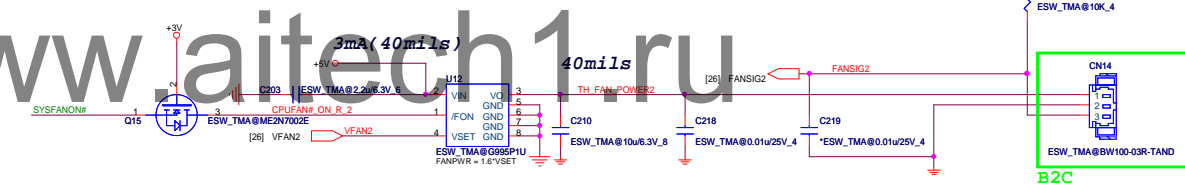


GA switchable control

[GSW]

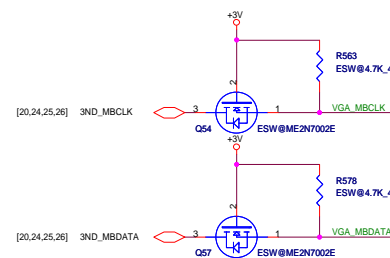
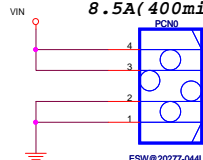


VGA FAN CTRL

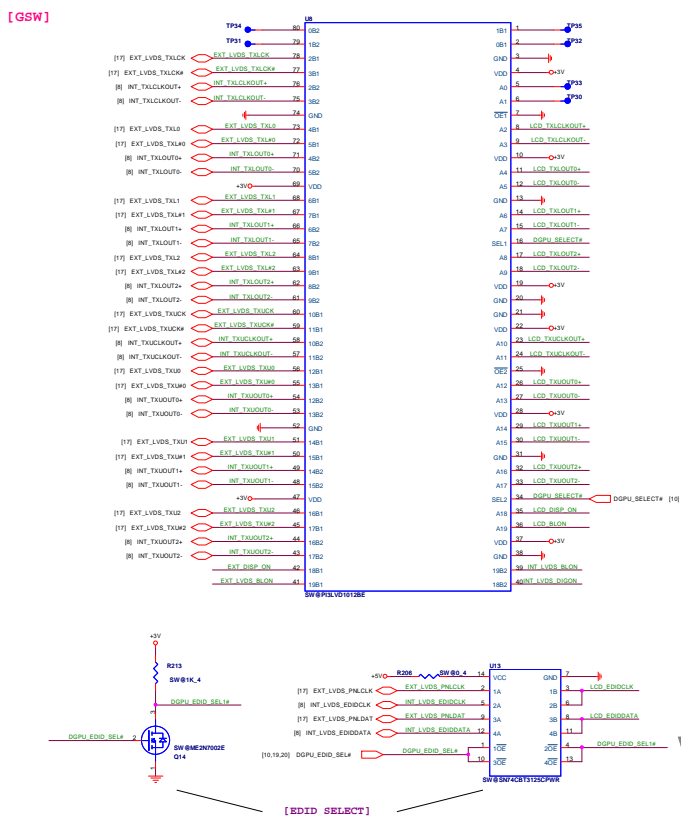


VGA Power conn

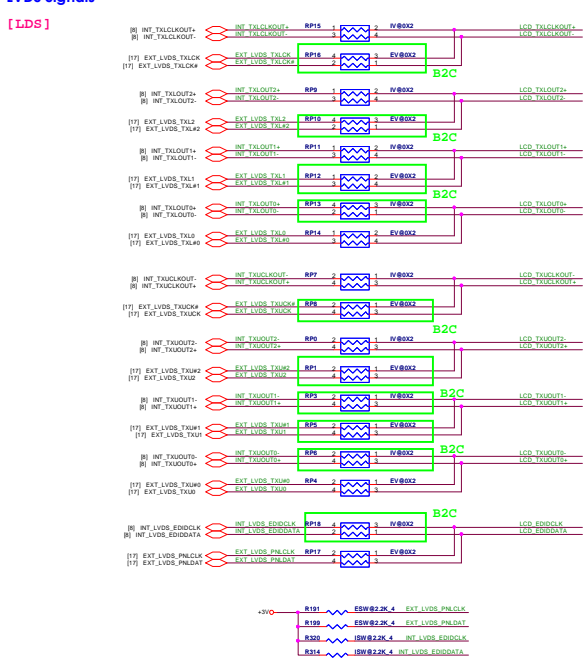
8.5A(400mils)



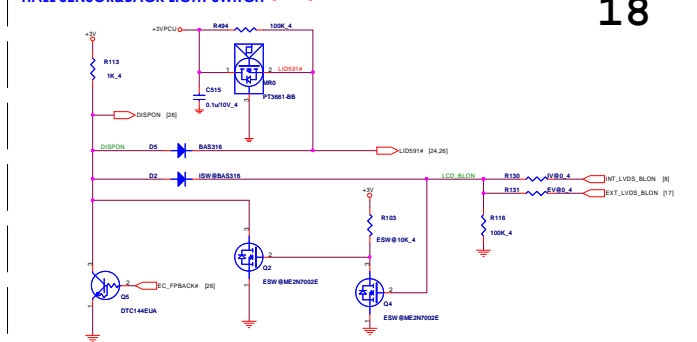
LVDS Signals [GSW]



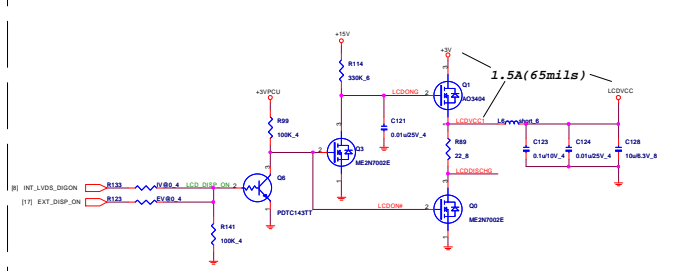
LVDS Signals [LDS]



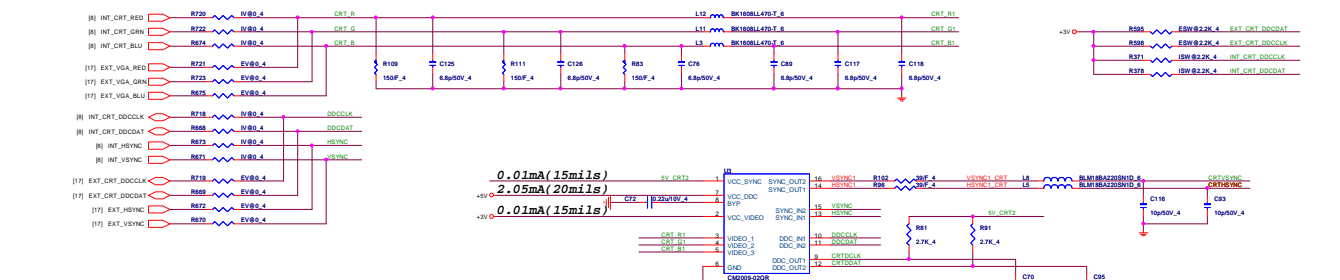
HALL SENSOR & BACK LIGHT SWITCH [HSR]



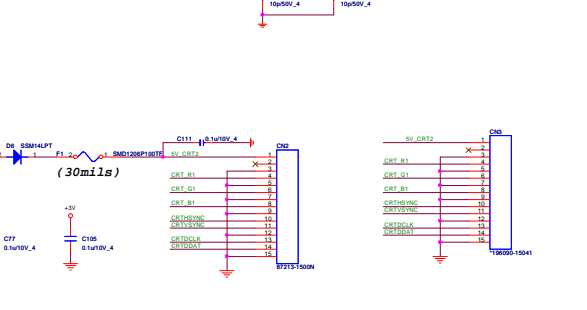
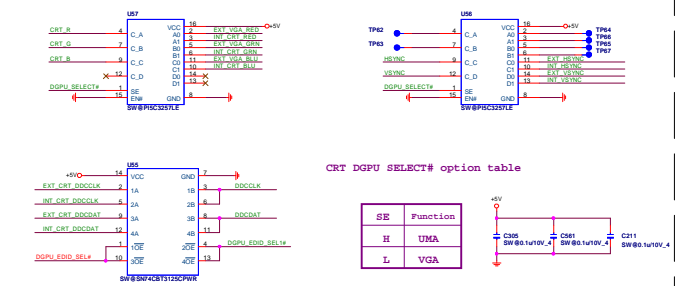
LCD POWER SWITCH [LDS]



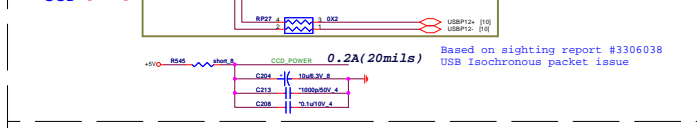
CRT [CRT]



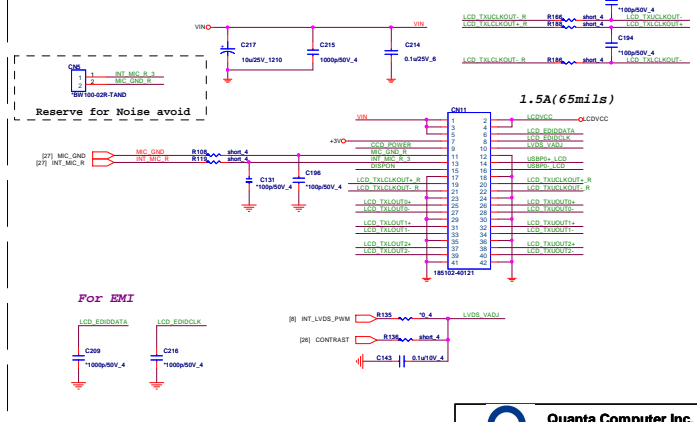
CRT Bus Switch [GSW]

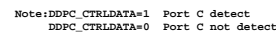


CCD [CCD]

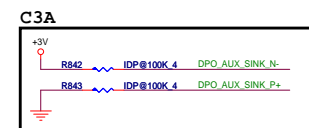
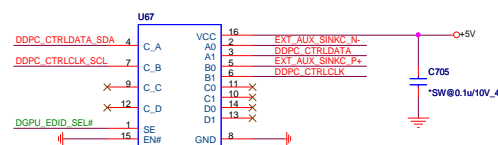


LCD Panel Module [LDS]

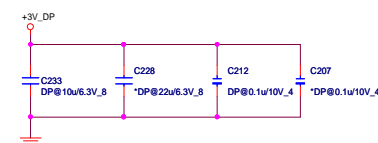
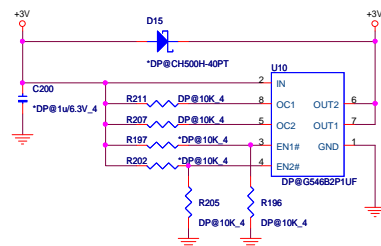




SE	Function
H	UMA
L	VGA



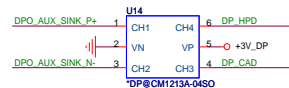
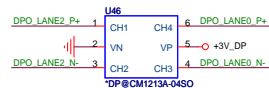
Based on DG. 1.6/ P.146
change PU/PD to Conn side



U44

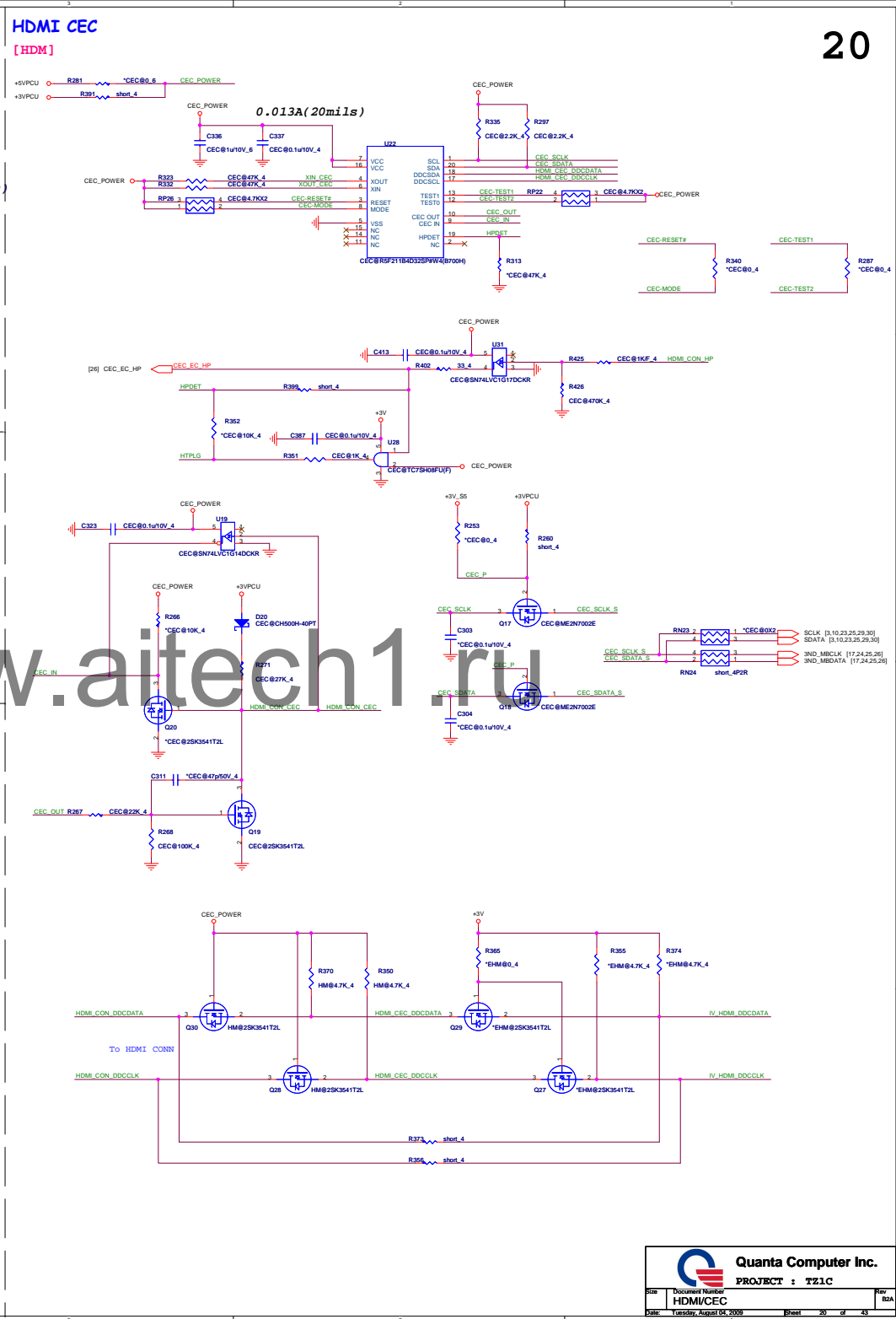
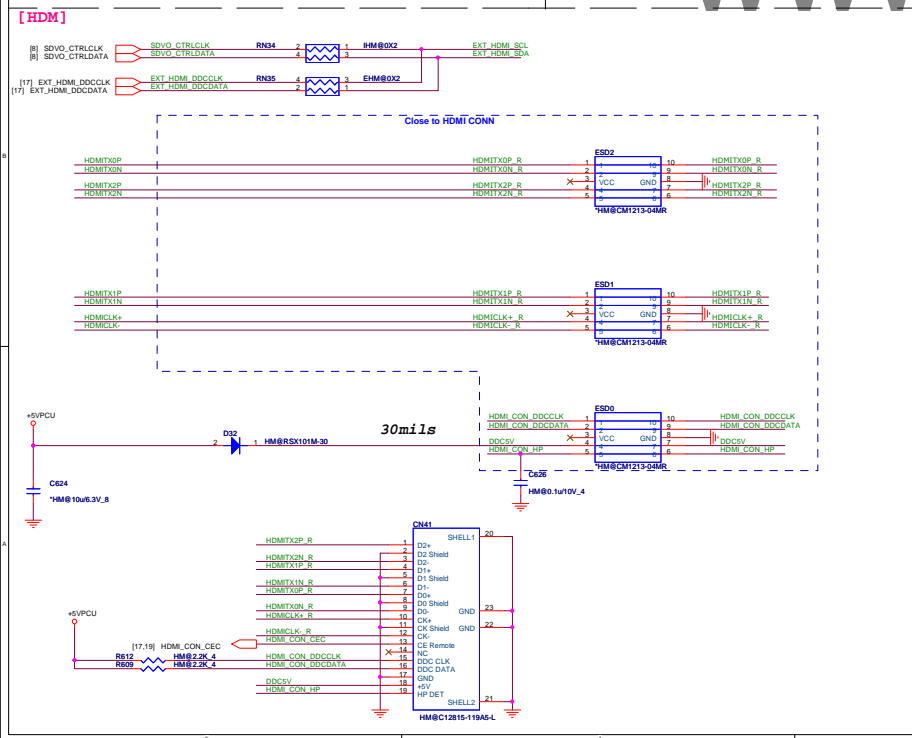
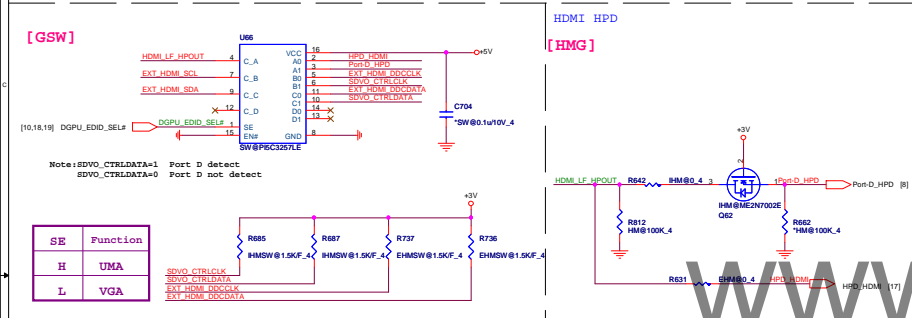
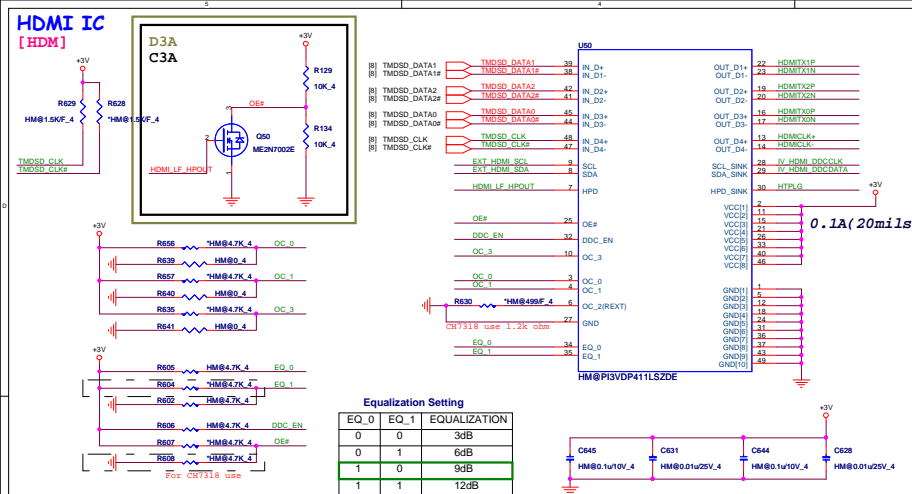
DPO_LANE1 P+	1	CH1	CH4	6	DPO_LANE3 P+
	2	VN	VP	5	+3V_DP
DPO_LANE1 N-	3	CH2	CH3	4	DPO_LANE3 N-

DP@CM1213A-04SO



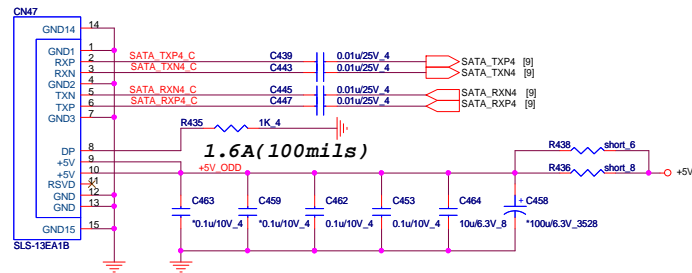
Close CONN





SATA ODD

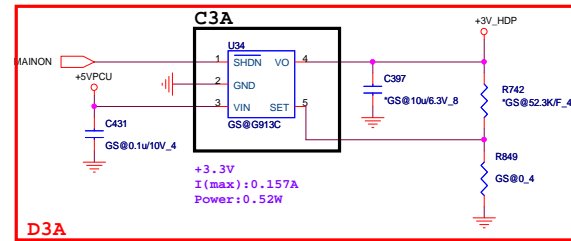
[ODD]



G-sensor

[H3D]

[12,17,26,35,36,37,38]



FS (Full Scale) selection

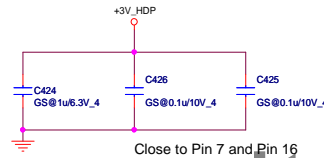
FS	0	1
2g Full-Scale		6g Full-Scale

PD (Power Down) selection

PD	0	1
Normal Mode		Power-down mode

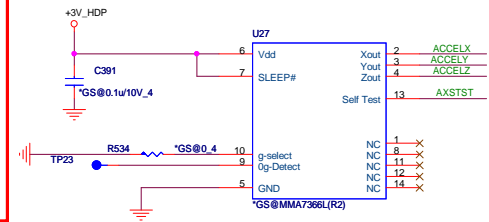
HDDPPD selection

HDDPPD	0	1
Normal Mode		Power-down mode



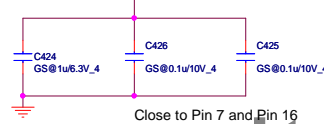
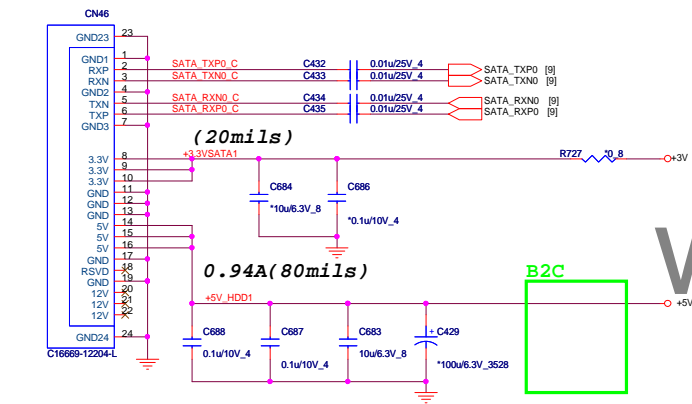
Close to Pin 7 and Pin 16

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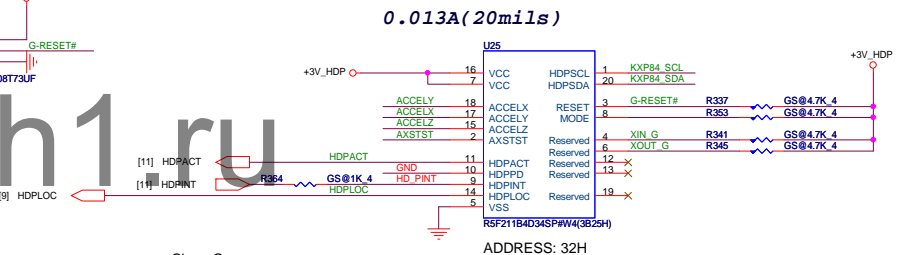
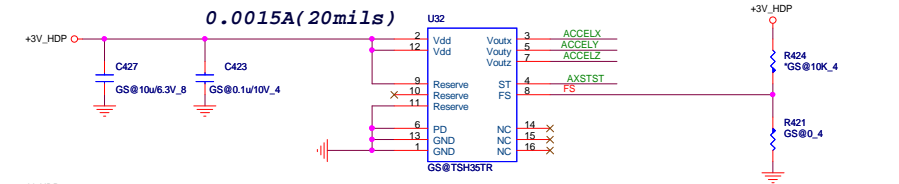


Main SATA HDD

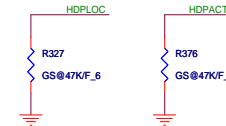
[HDD]



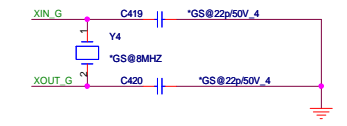
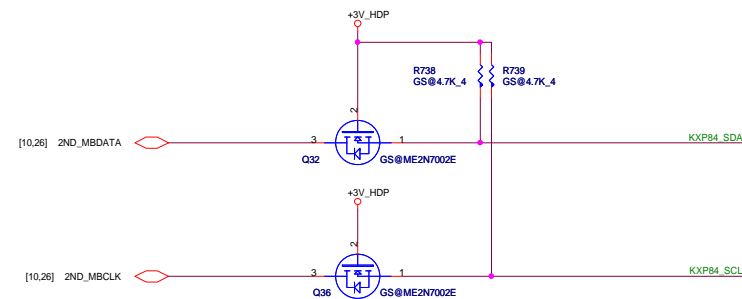
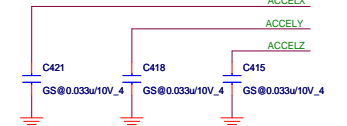
Close to Pin 7 and Pin 16



Close G-processor



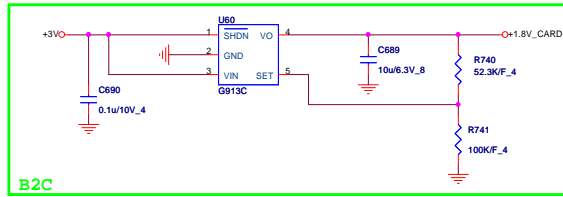
Close G-processor



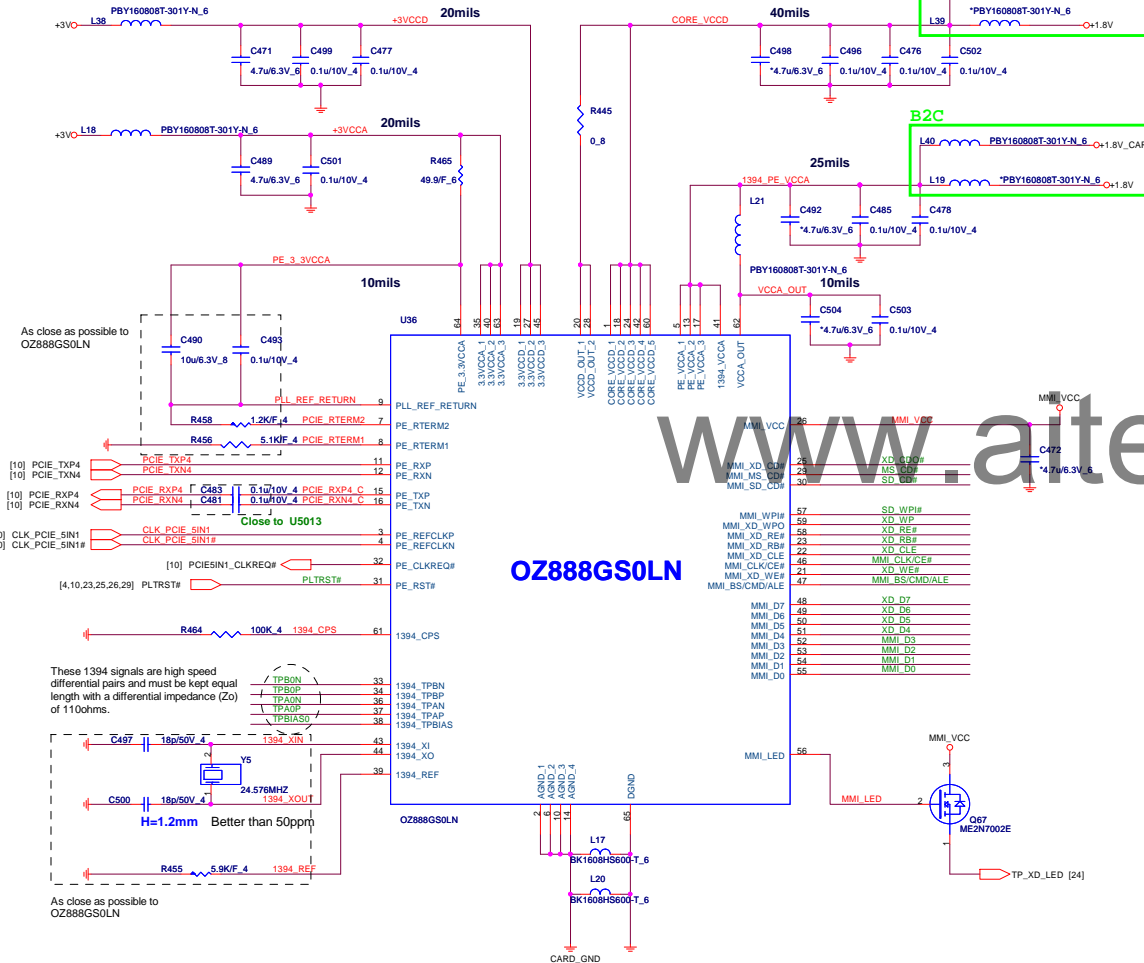
OZ888GS0LN

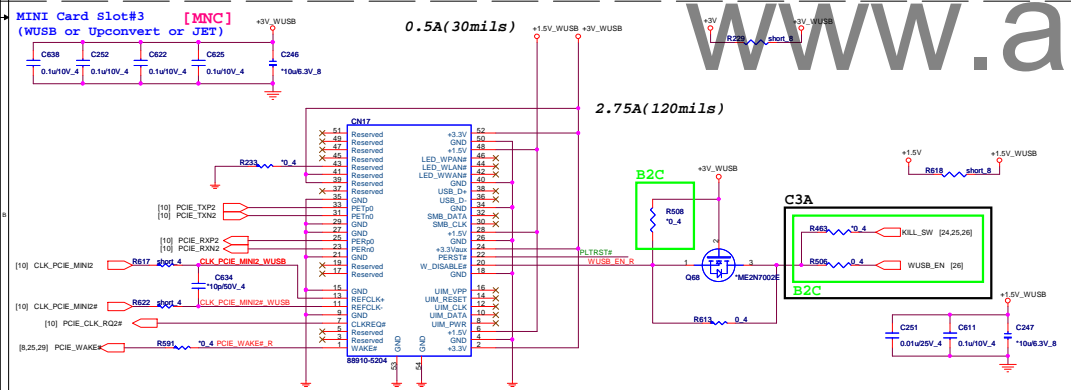
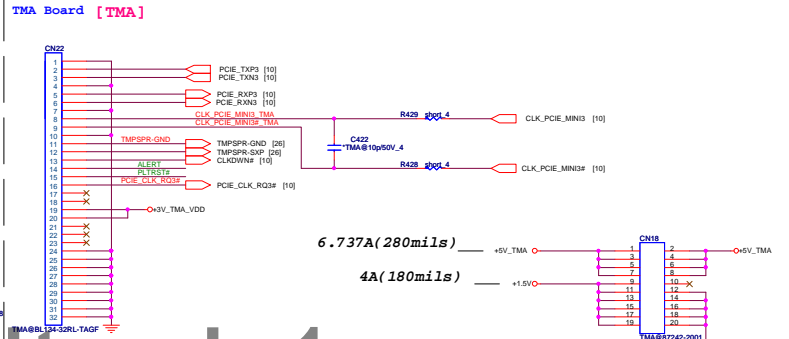
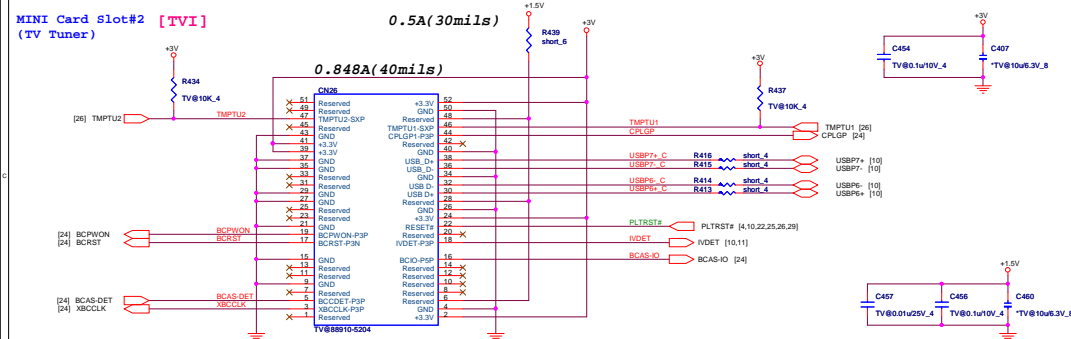
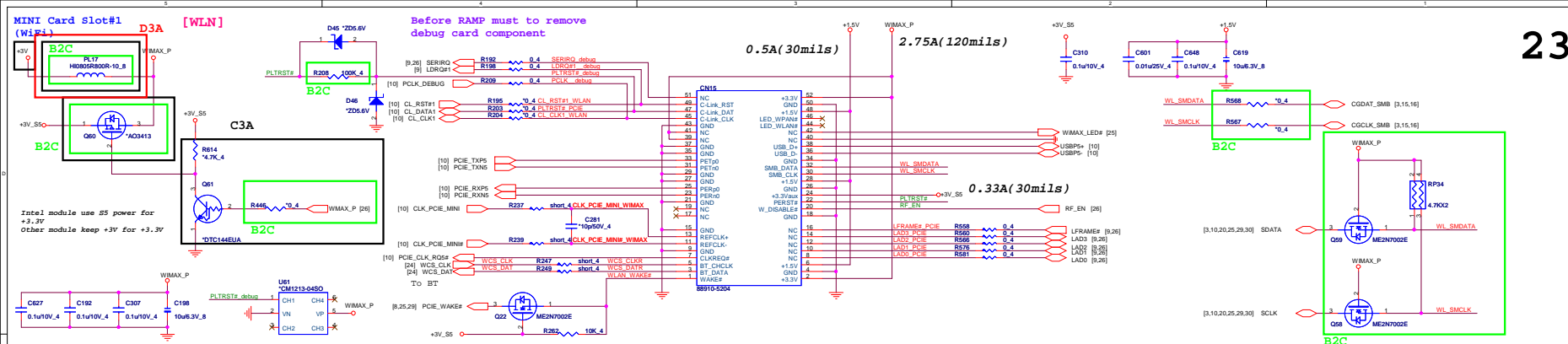
[MMC]

$$V_{out} = 1.25 [1 + (52.3/100)] = 1.903V$$

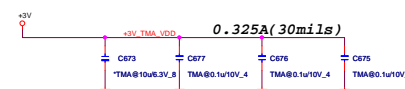


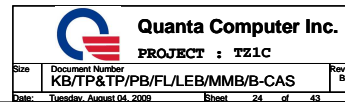
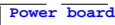
Each power pin is 100mA

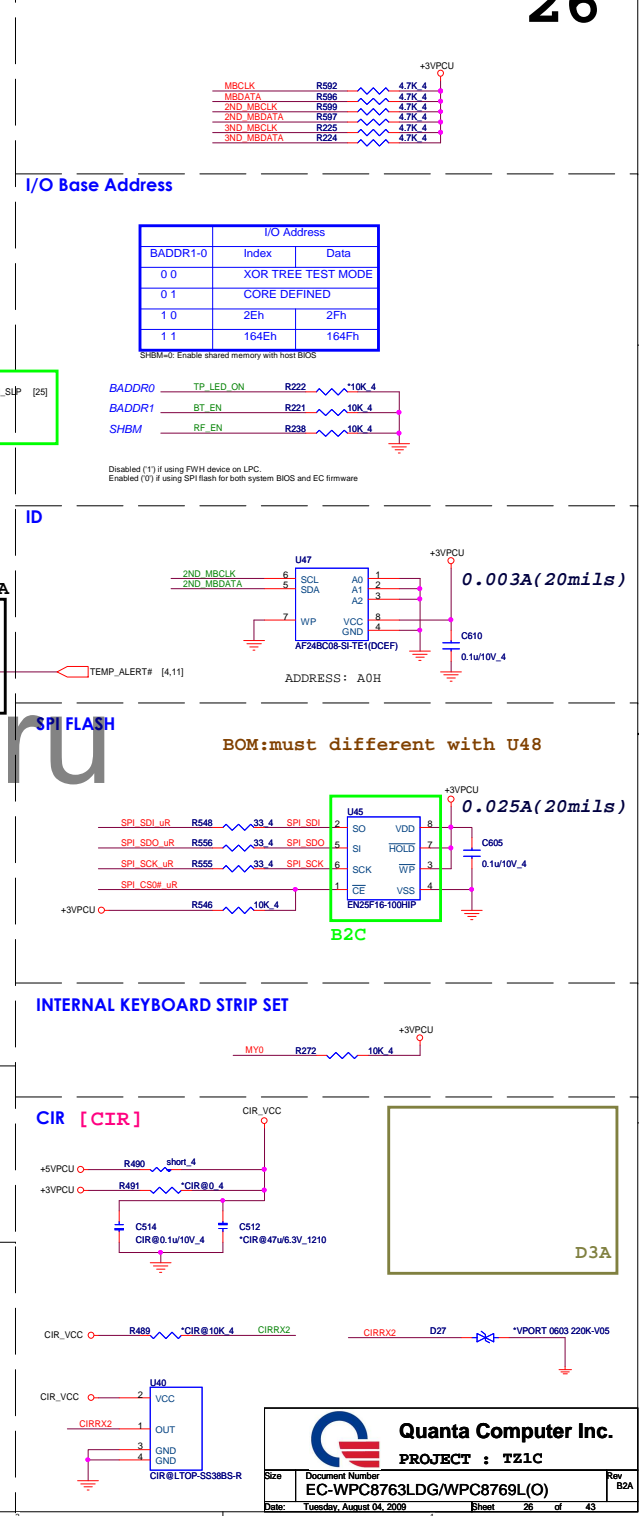
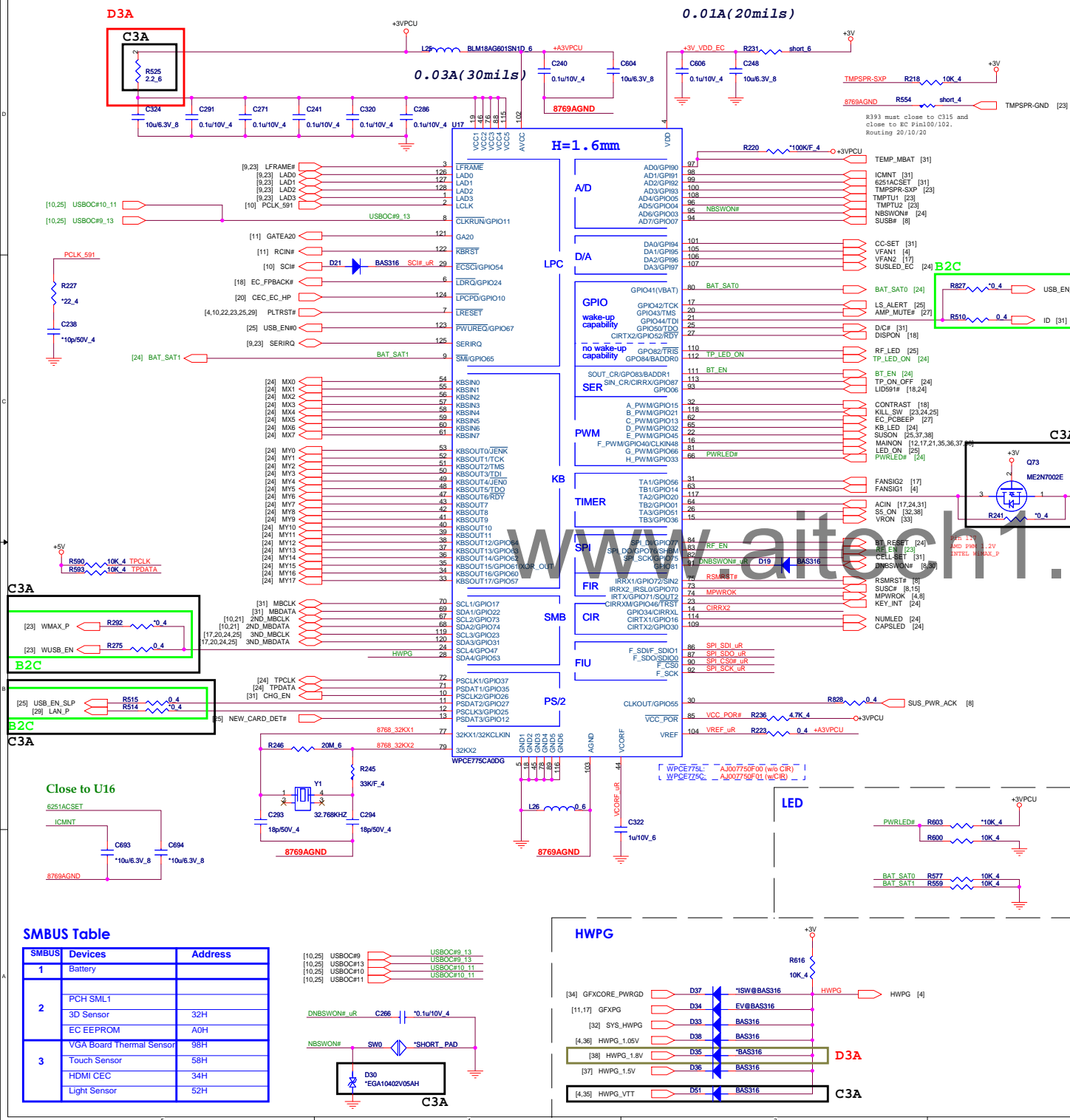


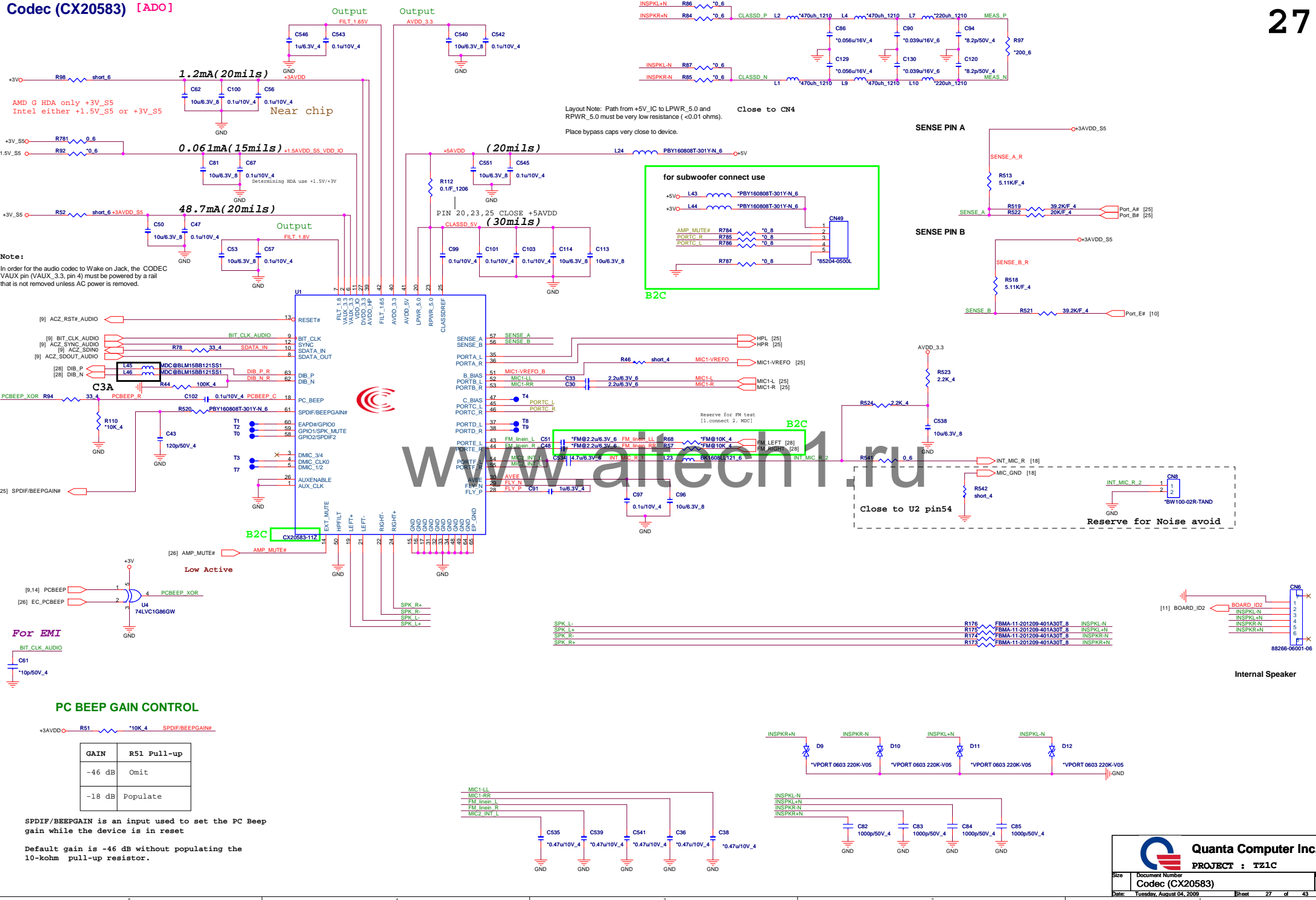


PCIe Mini Slot H=4	
Slot#1	WiFi
Slot#2	TV Tuner
Slot#3	WUSB or Upconvert or JET



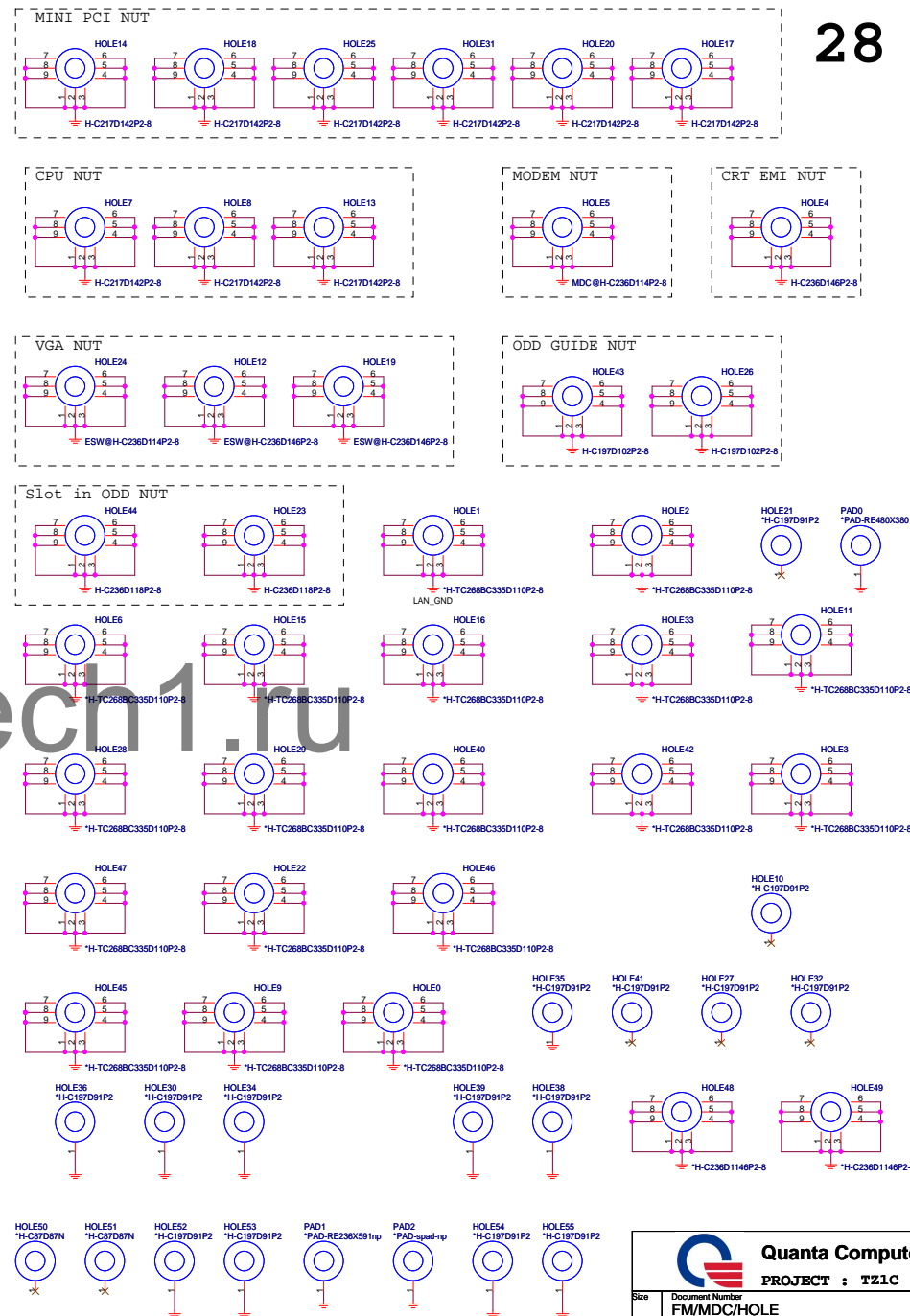




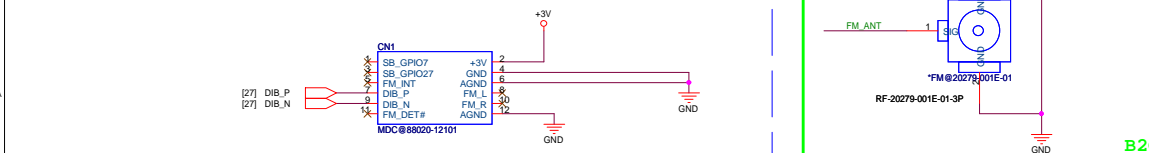
Codec (CX20583) [ADO]

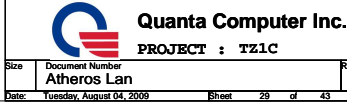
B2C	HOLE
-----	------

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B2C



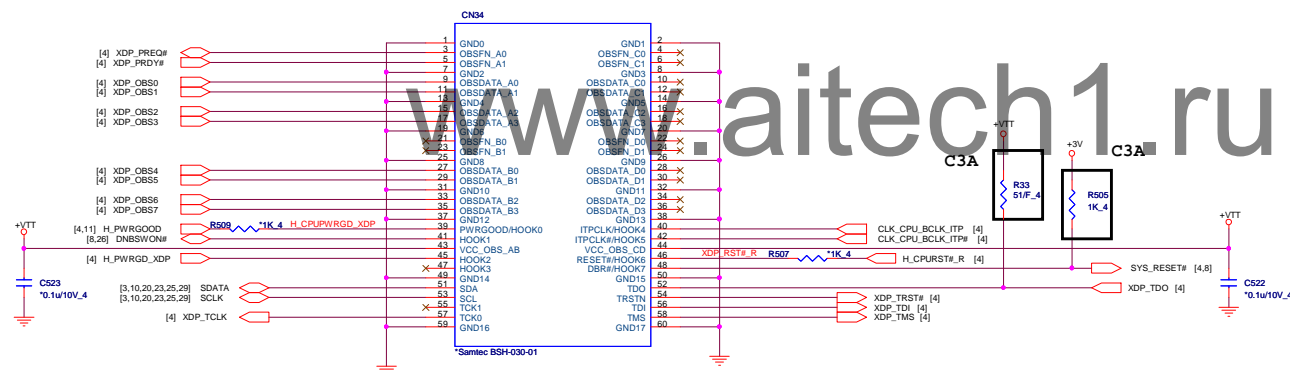


Feature Set	SKU Name (S)				
	Q57	H57	H55	P55	P57
BraidWood	Y	Y	N	N	Y

B2C

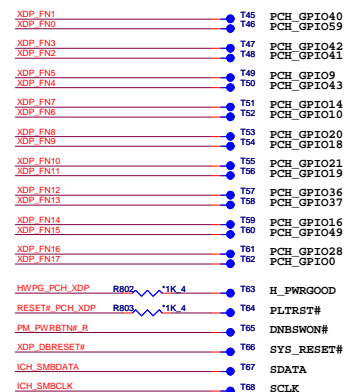
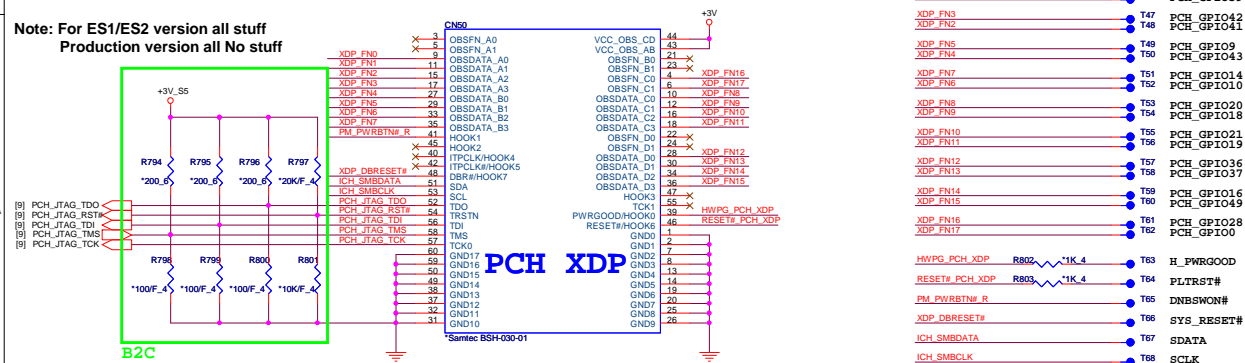
D3A

CPU XDP

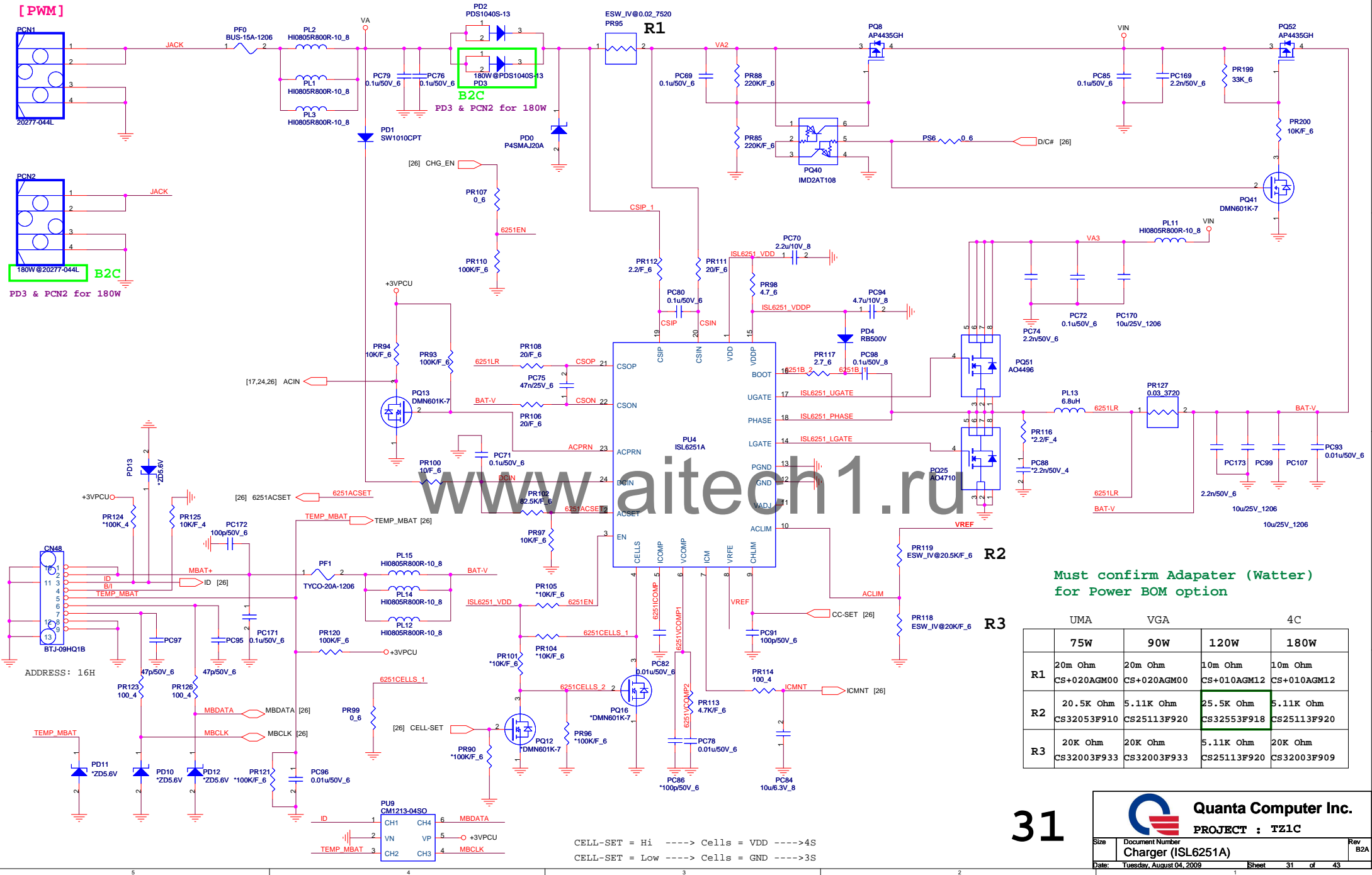


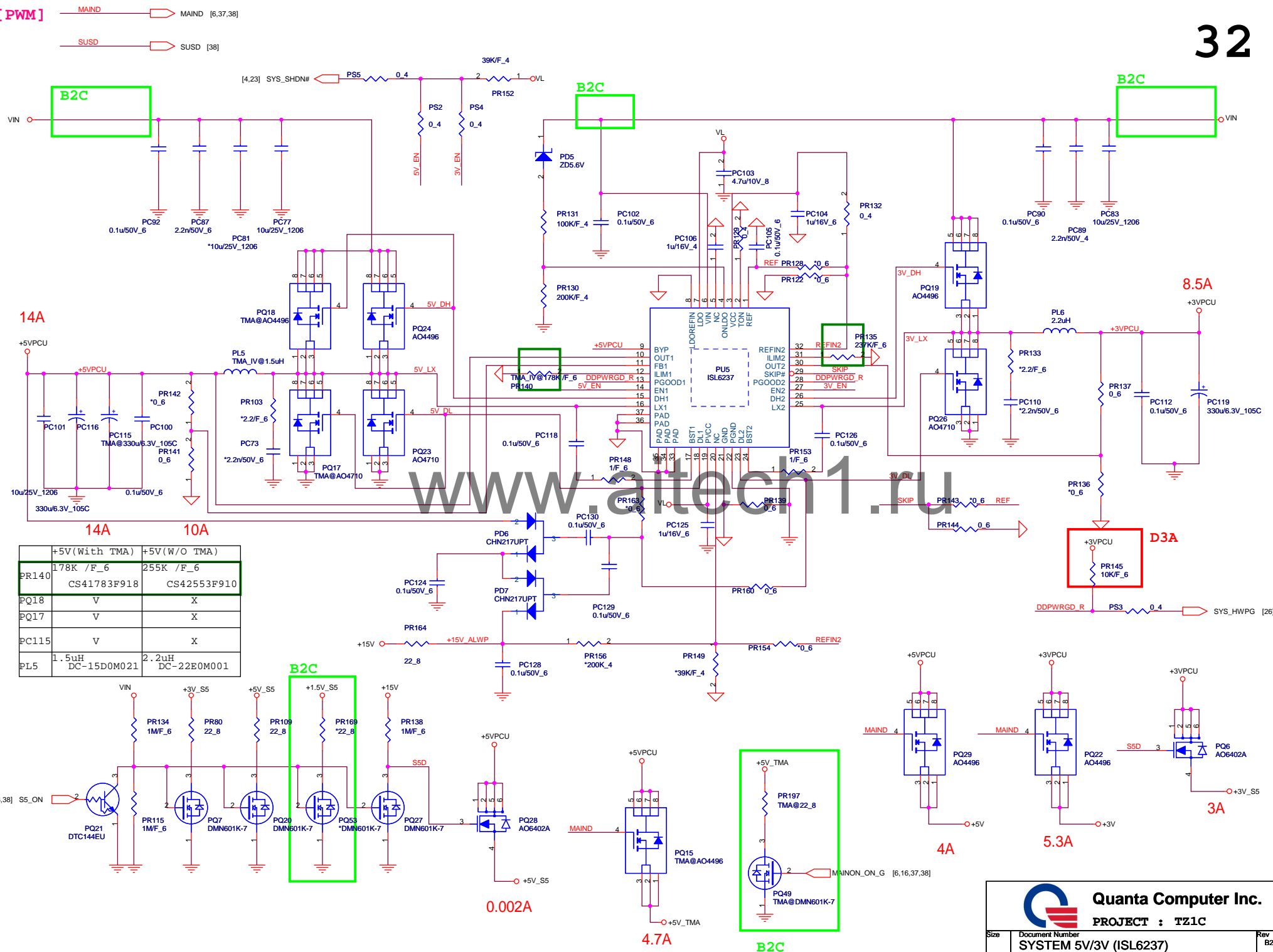
PCH XDP

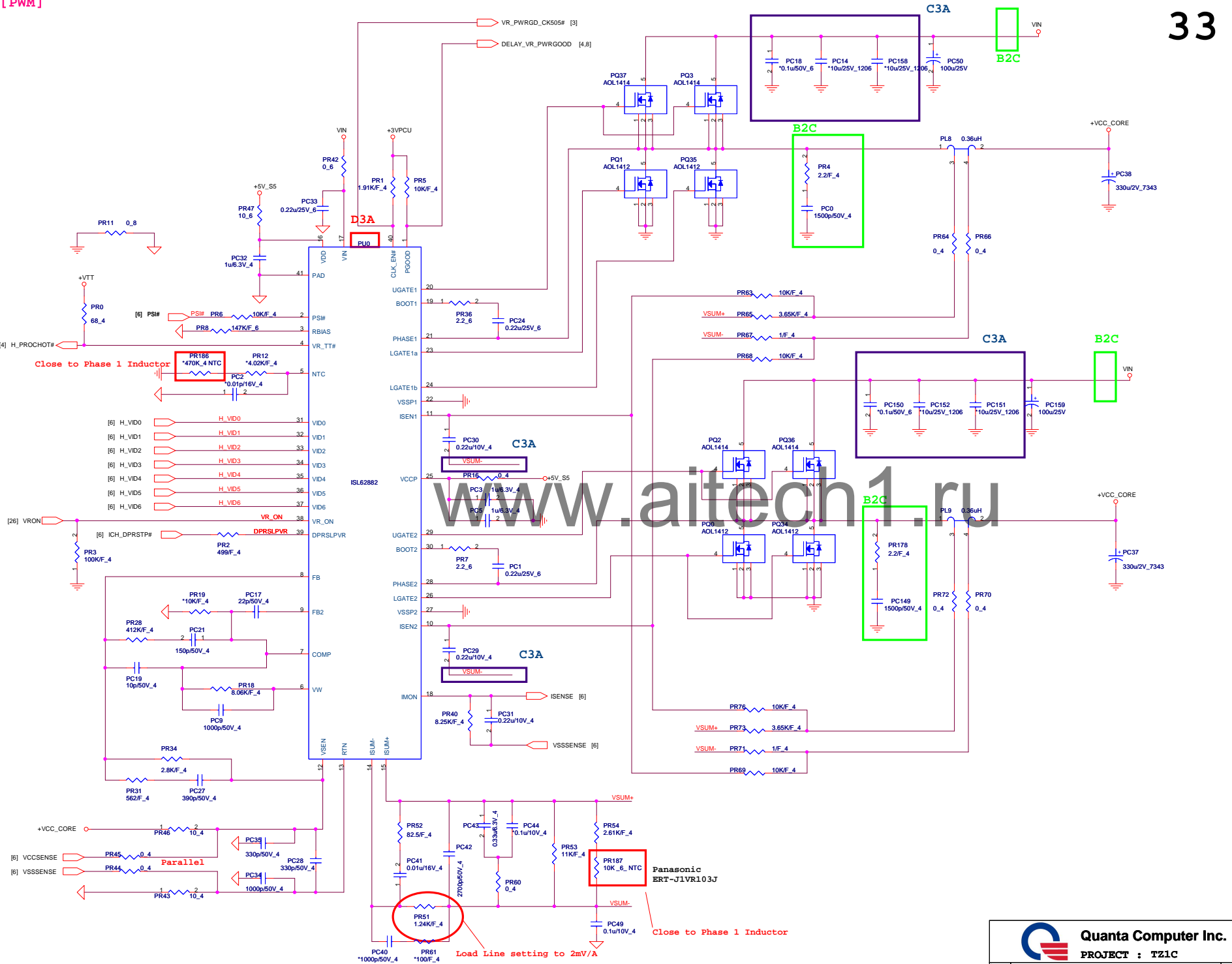
**Note: For ES1/ES2 version all stuff
Production version all No stuff**

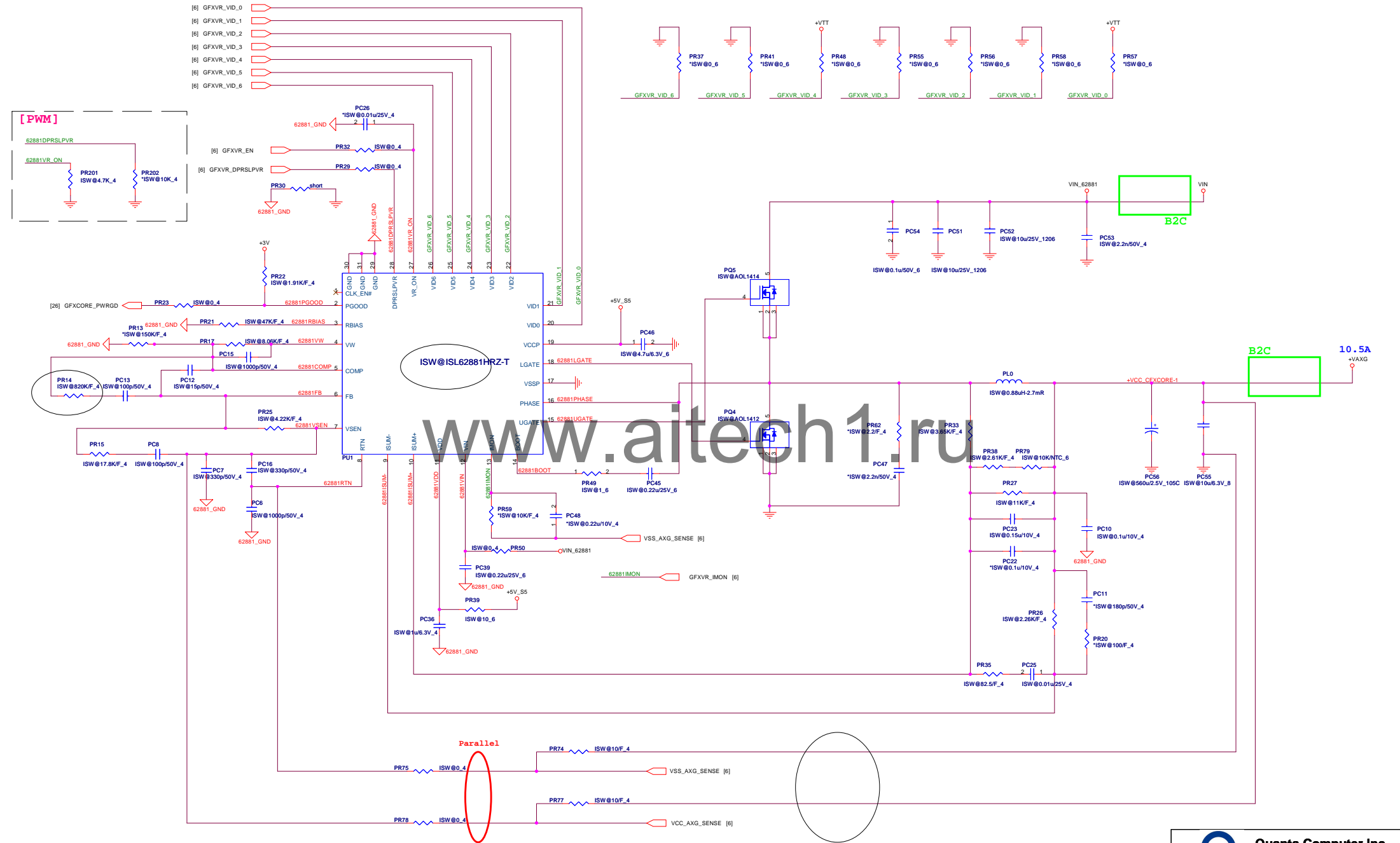


[PWM]



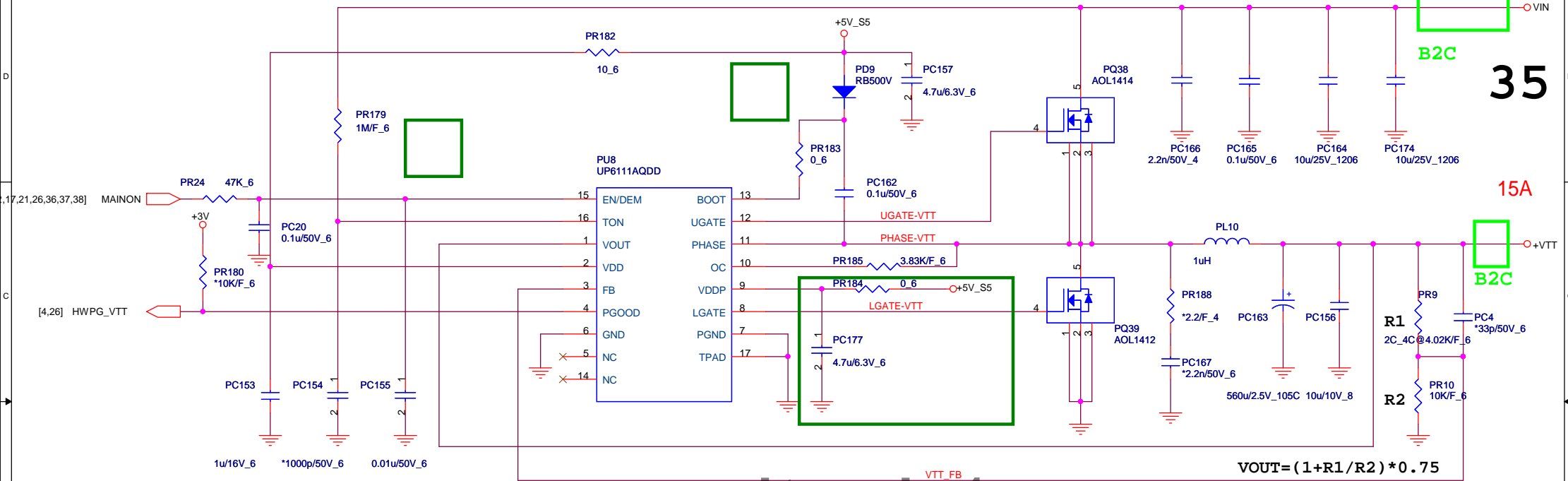






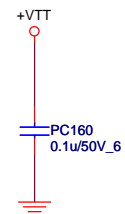
1. Level 1 Environment-related Substances should NEVER be used.
2. Purchase Ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

[PWM]



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Aurbundale (1.05V) R1 = 4.02K (CS24023F928)
 Clarksfield(1.1V) R1 = 4.75K (CS24753F919)

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[PWM]


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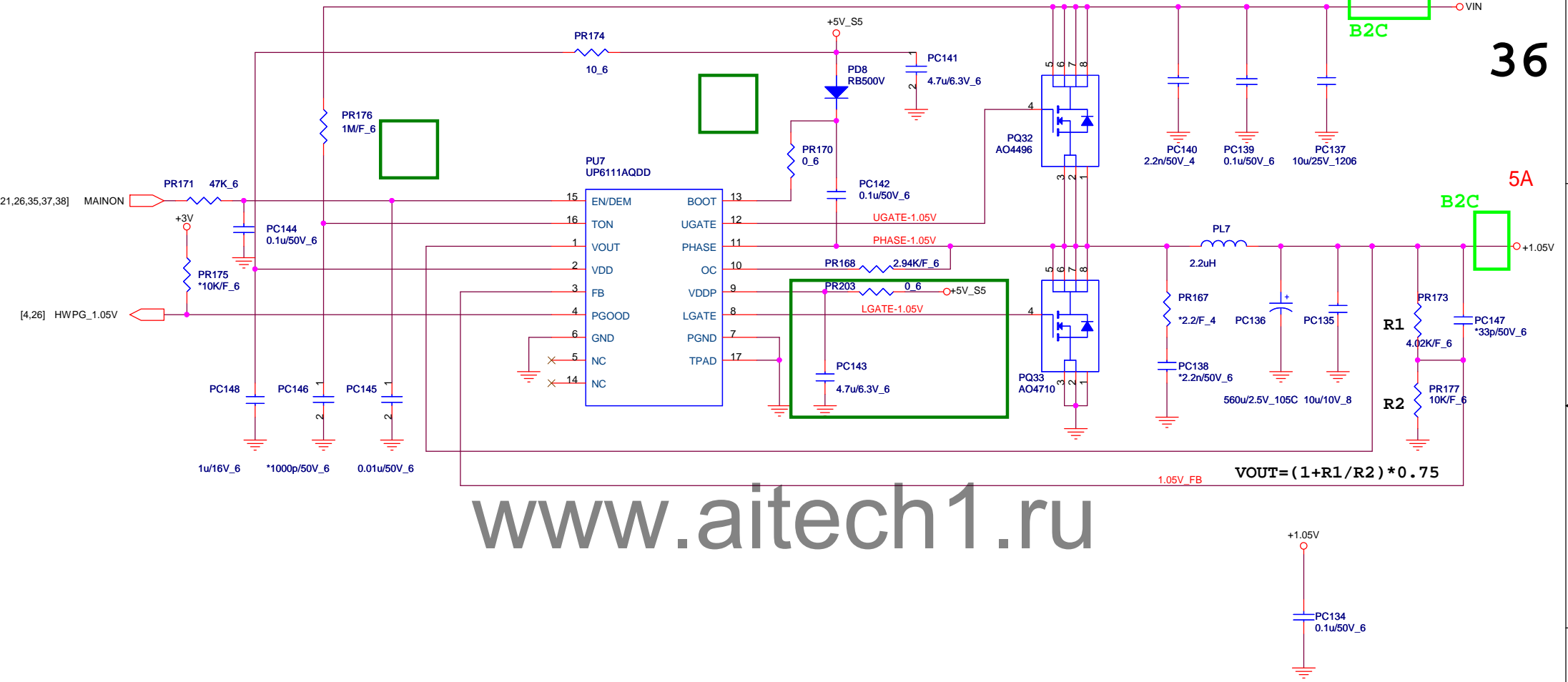
5A

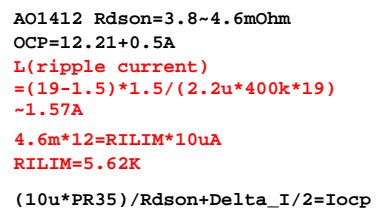
B2C

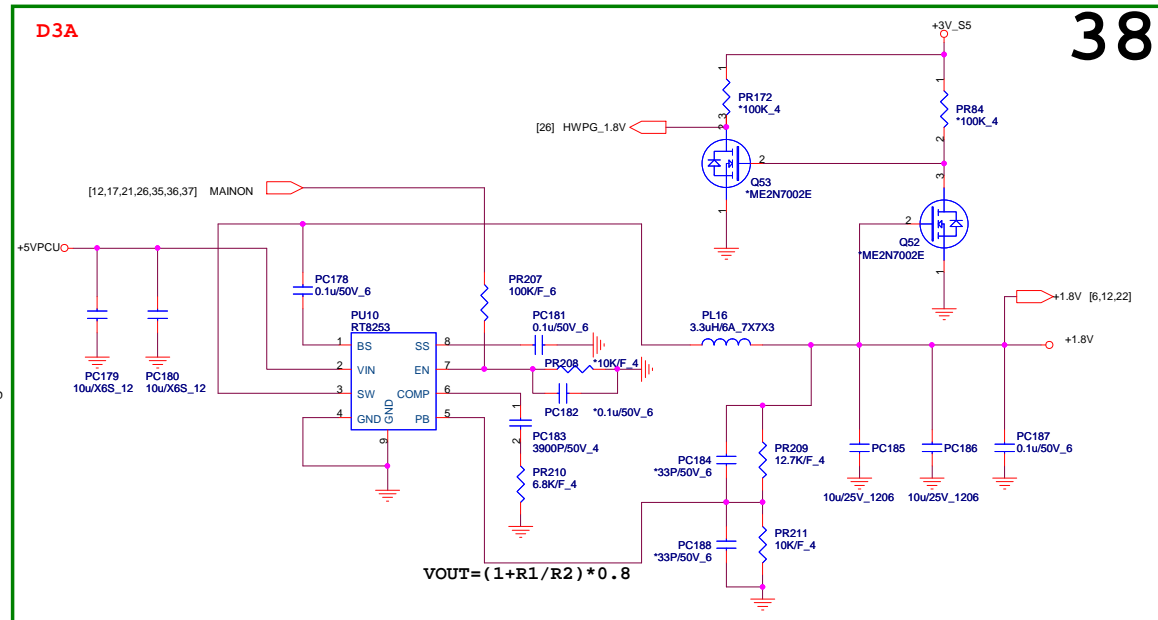
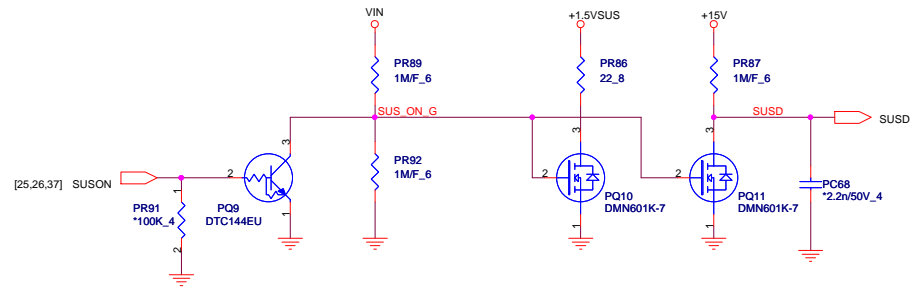
B2C

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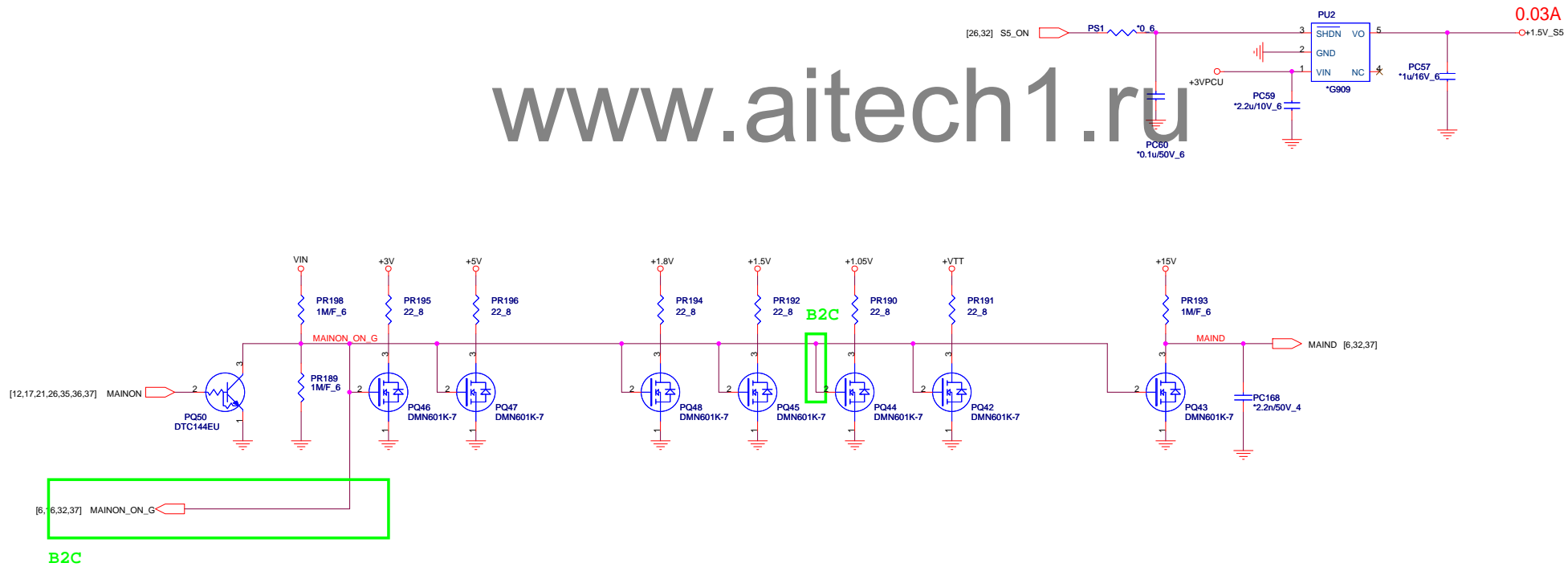
 Quanta Computer Inc. PROJECT : TZ1C	
Size	Document Number
+1.05V(UP6111AQDD)	
Date: Tuesday, August 04, 2009	Rev B2A



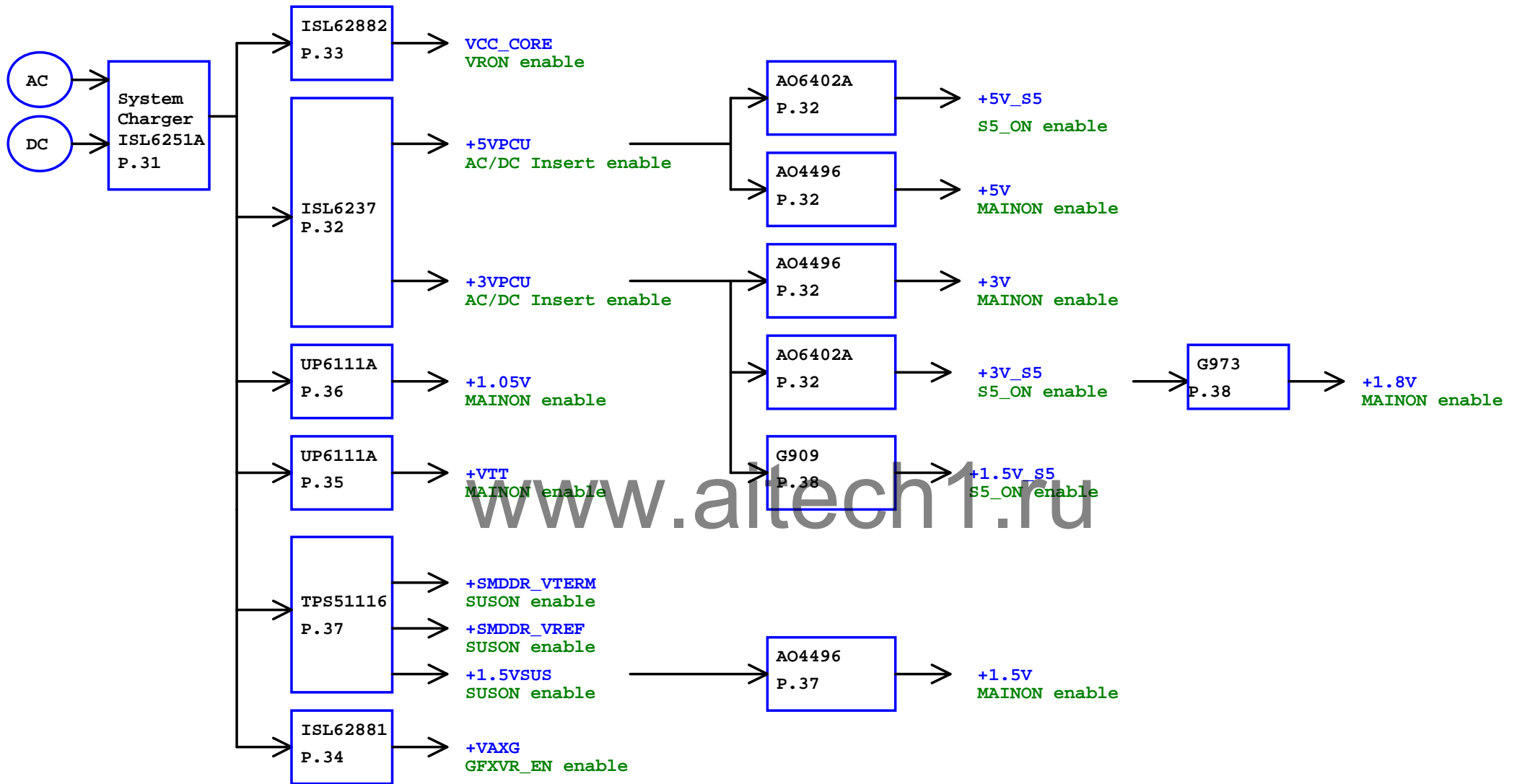




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Quanta Computer Inc.

PROJECT : TZ1C

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POWER TREE TABLE

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PCH POWER PLANE

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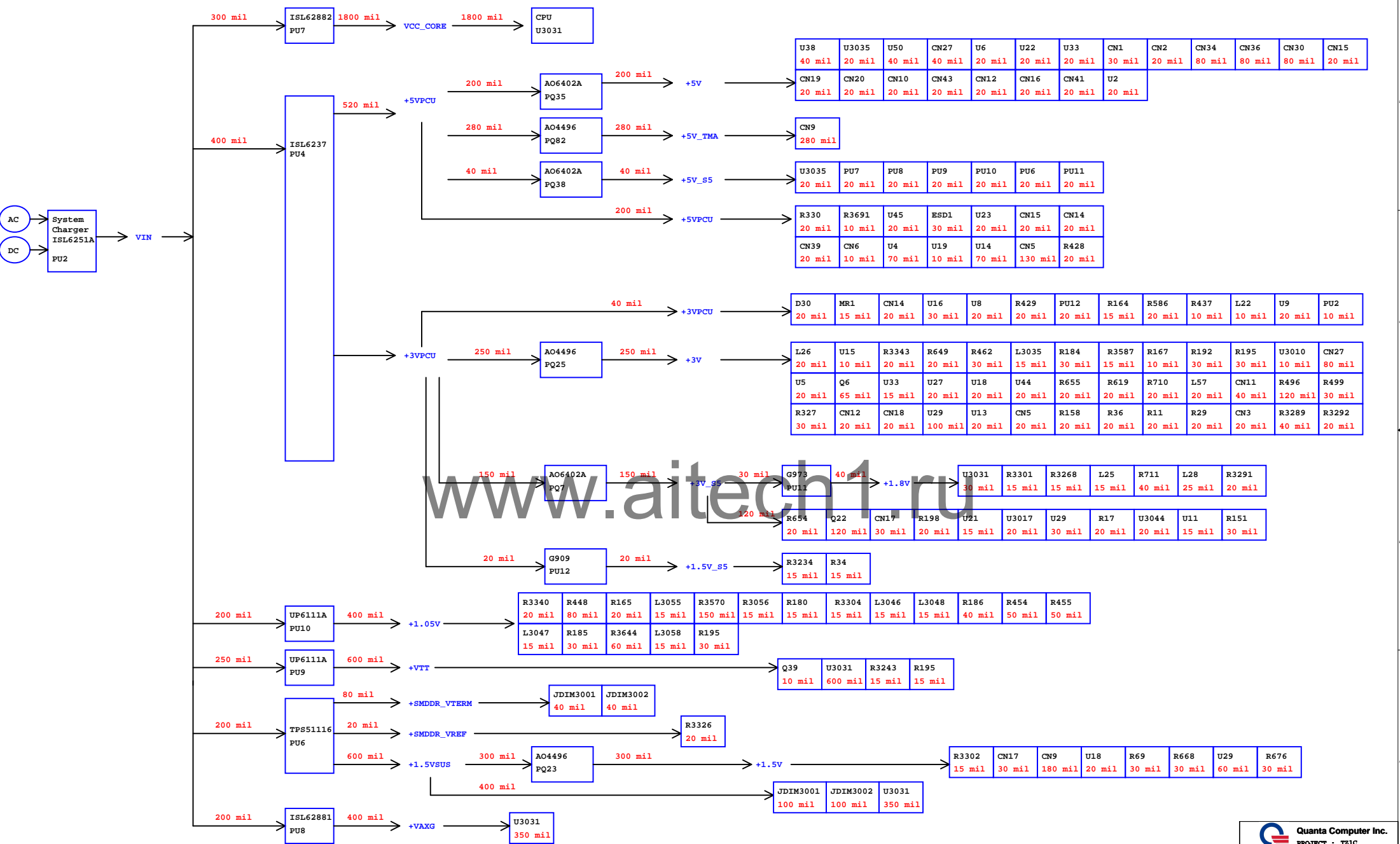
LOGIC	SUPPLY	LEVEL	S0	S3	S4	S5
Fast Flash	VccpNAND	+1.8V/+3.3V	ON	OFF	OFF	OFF
Core	DcpSusByp	+1.05V	ON	OFF	OFF	OFF
CPU	V_CPU_IO	+VTT	ON	OFF	OFF	OFF
PCI	V5REF	+5V/+3V	ON	OFF	OFF	OFF
USB	V5REF_Sus	+5V_S5/+3V_S5	ON	ON	ON	ON
DisplayPort, SATA, PCI	VCC3_3	+3V	ON	OFF	OFF	OFF
Core	VccCore	+1.05V	ON	OFF	OFF	OFF
PCIE/DMI	VccDMI	+VTT/+1.05V	ON	OFF	OFF	OFF
Fast Flash	VccME3_3	+3V	ON	OFF	OFF	OFF
PCIE/DMI,SATA,USB	VccIO	+1.05V	ON	OFF	OFF	OFF
Core	VccLAN	+1.05V	ON	OFF	OFF	OFF
Core	VccME	+1.05V	ON	OFF	OFF	OFF
RTC	VccRTC	+VCCRTC	ON	ON	ON	ON
USB&PCI	VccSus3_3	+3V_S5	ON	ON	ON	ON
IntelR HD Audio	VccSusHDA	+1.5V_S5	ON	ON	ON	ON
Core	VccVRM	+V1.5S_1.8S	ON	OFF	OFF	OFF
CLK	VccAClk	+1.05V	ON	OFF	OFF	OFF
CRT	VccADAC	+3V	ON	OFF	OFF	OFF
DPLL	VccADPLLA	+1.05V	ON	OFF	OFF	OFF
DPLL	VccADPLLb	+1.05V	ON	OFF	OFF	OFF
PCie/DMI	VccapIEXP	+1.05V	ON	OFF	OFF	OFF
IntelR FDI	VccFDIPLL	+1.05V	ON	OFF	OFF	OFF
SATA	VccSATAPLL	+1.05V	ON	OFF	OFF	OFF
Display	VccTX_LVDS	+1.8V	ON	OFF	OFF	OFF



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Model	REV	DATE	Change List	NOTE
TZ3	B2A	0223	First Release	
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